IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

LG.PHILIPS LCD CO., LTD., Plaintiff, v. CHI MEI OPTOELECTRONICS CORPORATION; CHI MEI OPTOELECTRONICS USA, INC.; AU OPTRONICS CORPORATION; AU OPTRONICS CORPORATION AMERICA; TATUNG COMPANY; TATUNG COMPANY OF AMERICA, INC.; AND VIEWSONIC CORPORATION, Defendants.	Civil Action No. 06-726-JJF DEMAND FOR TRIAL BY JURY

FIRST AMENDED COMPLAINT FOR PATENT INFRINGEMENT AGAINST DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION AND CHI MEI OPTOELECTRONICS USA, INC.

Plaintiff LG.Philips LCD Co., Ltd. ("LG.Philips") for its First Amended Complaint against Defendants Chi Mei Optoelectronics Corporation and Chi Mei Optoelectronics USA, Inc., and for its Complaint against AU Optronics Corporation; AU Optronics Corporation America; Tatung Company; Tatung Company of America, Inc.; and ViewSonic Corporation (collectively the "Defendants") for injunctive and declaratory relief and for damages, including treble or multiple damages, for patent infringement, states and alleges as follows:

NATURE OF THE ACTION

1. LG.Philips is the owner of United States Patent No. 5,019,002 ("the '002 Patent"), United States Patent No. 5,825,449 ("the '449 Patent"), and United States Patent No. 4,624,737 ("the '737 Patent") (collectively the "Patents-in-Suit").

2. Chi Mei Optoelectronics Corporation claims to be the owner by assignment of United States Patent No. 6,008,786 ("the '786 Patent"), United States Patent No. 6,013,923 ("the '923 Patent"), United States Patent No. 5,619,352 ("the '352 Patent"), and United States Patent No. 6,734,926 B2 ("the '926 Patent") (collectively "the Chi Mei Patents").

3. This is a civil action for the infringement of the Patents-in-Suit, including the willful infringement of the Patents-in-Suit by Defendants, and for a declaration of invalidity and non-infringement of the claims of the Chi Mei Patents.

4. The technology at issue involves the design and manufacture of Liquid Crystal Display modules ("LCDs"), which are a type of flat panel display that are incorporated into at least LCD portable computers, LCD computer monitors, and LCD televisions.

THE PARTIES

5. Plaintiff LG.Philips is a corporation organized under the laws of the Republic of Korea, having a place of business located in Seoul, Korea.

6. Defendant Chi Mei Optoelectronics Corporation ("Chi Mei") is a Taiwanese corporation, having its principal place of business at 2F, No. 1, Chi-Yeh Road, Tainan Science Based Industrial Park, Hsinshih Hsiang, Tainan Hsien 710, TAIWAN 74147, R.O.C. Chi Mei manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

7. Defendant Chi Mei Optoelectronics USA, Inc. ("Chi Mei USA") is a domestic subsidiary of Chi Mei that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. Chi Mei owns 100% of the shares of Chi Mei Optoelectronics Japan Co., Ltd. ("Chi Mei Japan"), which in turn owns 100% of the shares of Chi Mei USA. Chi Mei USA is a Delaware corporation, having its principal pace of business at 101 Metro Drive Suite 510, San Jose, CA 95110. Chi Mei USA markets and sells Chi Mei's products throughout the United States.

8. Defendant AU Optronics Corporation ("AUO") is a Taiwanese corporation, having its principal place of business at 1, Li-Hsin Rd., II, Science-Based Industrial Park, Hsinchu City 30077 Taiwan, ROC. AUO manufactures LCD products in Taiwan and China and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

9. Defendant AU Optronics Corporation America a/k/a AU Optronics America, Inc. ("AUO America") is a domestic subsidiary of AUO that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. AUO America is a California corporation, having its principal place of business at 1800 Wyatt Drive, Suite 7, Santa Clara, CA 95054. AUO America markets and sells AUO's products throughout the United States.

10. Defendant Tatung Company ("Tatung") is a Taiwanese corporation, having a place of business at 22 Chungshan N Rd. Section 3, Taipei, Taiwan. Tatung assembles LCD

products in Taiwan and, on information and belief, directs those products to the United States, including Delaware, through established distribution channels involving various third parties, knowing that these third parties will use their respective nationwide contacts and distribution channels to import into, sell, offer for sale, and/or use these products in Delaware and elsewhere in the United States.

11. Defendant Tatung Company of America, Inc. ("Tatung America") is a domestic subsidiary of Tatung that either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States. Tatung America is a California corporation, having a place of business at 2850 El Presidio Street, Long Beach, California 90810. Tatung America markets and sells Tatung's products throughout the United States.

12. Defendant ViewSonic Corporation ("ViewSonic") is a Delaware Corporation, having a place of business at 381 Brea Canyon Road, Walnut, California 91789, which either directly or indirectly imports into, sells, and/or offers for sale its products in Delaware and elsewhere in the United States,

JURISDICTION AND VENUE

13. This action is based upon and arises under the Patent Laws of the United States, 35 U.S.C. § 100 *et seq*., and in particular §§ 271, 281, 283, 284 and 285, and is intended to redress infringement of the Patents-in-Suit owned by LG.Philips.

14. This Court has jurisdiction over the subject matter of this action pursuant to 28 U.S.C. §§ 1331 and 1338(a).

15. Additionally, this action is under the Declaratory Judgment Act, 28 U.S.C. §§ 2201 and 2202, and the Patent Laws of the United States, based upon an actual controversy

between LG.Philips and Chi Mei regarding the validity and infringement of the claims of the Chi Mei Patents, and is intended to provide appropriate and necessary declaratory relief.

16. Defendants have transacted and continue to transact business in the United States and in this judicial district by: using or causing to be used; making; importing or causing to be imported; offering to sell or causing to be offered for sale; and/or selling or causing to be sold directly, through intermediaries and/or as an intermediary, a variety of products that infringe the Patents-in-Suit to customers in the United States, including customers in this judicial district, and Defendants will continue to do so unless enjoined by this Court.

17. This Court has personal jurisdiction over Chi Mei, AUO, and Tatung, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c) and (d), and 28 U.S.C. § 1400(b), in that these Defendants are committing and are causing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary, and in that these Defendants have caused and cause injury and damages in this judicial district by acts or omissions outside of this judicial district, including but not limited to utilization of their own distribution channels established in the United States and Chi Mei USA's, AUO America's, and Tatung America's distribution channels in the United States, as set forth below, to ship a variety of products that infringe the Patents-in-Suit into the United States and into this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

18. This Court has personal jurisdiction over AUO America and Tatung America and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that these Defendants are committing acts of patent infringement within the United

States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and as an intermediary. AUO America and Tatung America regularly import large quantities of AUO, and Tatung LCD products into the United States for distribution throughout the United States, including in this judicial district. AUO America and Tatung America are involved in the distribution of infringing LCD products and are aware that their products are sold throughout the United States, including in Delaware. The established distribution networks of these Defendants consist of national distributors and resellers, and these Defendants distribute to national retailers that have stores located in Delaware. By shipping into, offering to sell in, using, or selling products that infringe the Patents-in-Suit in this judicial district, or by inducing or causing those acts to occur, AUO America and Tatung America have transacted and transact business and perform works and services in this judicial district, have contracted and contract to supply services and things in this judicial district, have caused and cause injury and damages in this judicial district by acts and omissions in this judicial district, and have caused and cause injury and damages in this judicial district by acts or omissions outside of this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

19. This Court has personal jurisdiction over Chi Mei USA, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that Chi Mei USA is incorporated and therefore resides in Delaware for purposes of establishing venue in this district, in that Chi Mei USA has been doing business in Delaware and is committing acts of patent infringement within the United States and within this judicial district, including the infringing acts alleged herein, both directly, through one or more intermediaries, and/or as an intermediary. Chi Mei USA regularly imports large quantities of Chi Mei LCD

products into the United States for distribution throughout the United States, including in this judicial district. Chi Mei USA is involved in the distribution of infringing LCD products and is aware that its products are sold throughout the United States, including in Delaware. The established distribution networks of Chi Mei USA consist of national distributors and resellers, and Chi Mei USA distributes to national retailers that have stores located in Delaware. By shipping into, offering to sell in, using, or selling products that infringe the Patents-in-Suit in this judicial district, or by inducing or causing those acts to occur, Chi Mei USA has transacted and transacts business and performs works and services in this judicial district, has contracted and contracts to supply services and things in this judicial district, has caused and causes injury and damages in this judicial district by acts and omissions in this judicial district, and has caused and causes injury and damages in this judicial district by acts or omissions outside of this judicial district while deriving substantial revenue from services or things used or consumed within this judicial district, and will continue to do so unless enjoined by this Court.

20. This Court has personal jurisdiction over ViewSonic, and venue is proper in this judicial district pursuant to 28 U.S.C. §§ 1391 (b) and (c), and 28 U.S.C. § 1400(b), in that ViewSonic is incorporated and therefore resides in Delaware for purposes of establishing venue in this district, in that ViewSonic has been doing business in Delaware, including the infringing acts alleged herein, both directly, through one or more intermediaries, and/or as an intermediary, and will continue to do so unless enjoined by this Court.

THE PATENTS-IN-SUIT

21. On May 28, 1991, the ‘002 Patent, entitled “Method of Manufacturing Flat Panel Backplanes including Electrostatic Discharge Prevention and Displays Made Thereby,” was duly

and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '002 Patent. A copy of the '002 Patent is attached as Exhibit A.

22. On October 20, 1998, the '449 Patent, entitled "Liquid Crystal Display Device and Method of Manufacturing the Same," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '449 Patent. A copy of the '449 Patent is attached as Exhibit B.

23. On November 25, 1986, the '737 Patent, entitled "Process for Producing Thin-Film Transistor," was duly and legally issued. LG.Philips is the owner by assignment of all rights, title, and interest in and to the '737 Patent. A copy of the '737 Patent is attached as Exhibit C.

24. LG.Philips owns the Patents-in-Suit and possesses the right to sue and to recover for infringement of the Patents-in-Suit.

25. Defendants have been and are infringing and/or inducing infringement of the Patents-in-Suit because they at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in this judicial district and elsewhere in the United States products that infringe the Patents-in-Suit.

FACTUAL BACKGROUND

26. LG.Philips has invested substantial time and money in designing, developing, manufacturing and producing LCD products that incorporate the patented LCD technology.

27. LG.Philips derives substantial benefits from the exploitation of its patented technology in the United States and abroad. LG.Philips' interests, including, but not limited to,

these benefits have been and continue to be harmed by the Defendants' infringement of the Patents-in-Suit.

28. The Defendants at least use, cause to be used, make, import, cause to be imported, offer for sale, cause to be offered for sale, sell, and/or cause to be sold in the United States and in this judicial district LCDs and/or LCD products that are encompassed by and/or made by the methods claimed in the Patents-in-Suit.

29. The Defendants have induced and/or continue to induce the infringement of the Patents-in-Suit in the United States and in this judicial district.

30. Defendants maintain and develop relationships with business partners, including, for example, suppliers and customers, to promote and encourage the import, offering for sale, sale and use of its infringing visual display products in the United States.

31. Defendants actively sell to and solicit business from customers and distributors located in the United States. Defendants coordinate with these and other third parties concerning the designs, specifications, distribution and/or placement of orders regarding such LCDs and LCD products destined for the U.S. market.

32. Defendants also communicate with third parties to promote and encourage the use, sale, importation and/or offering for sale of these same LCDs and LCD products in and into the United States.

33. Defendants have relationships with third parties to develop and supply the U.S. market with such LCDs and LCD products.

34. Defendants communicate and meet with third parties about their LCDs and LCD products and these communications and meetings facilitate the sale, offer for sale and/or distribution of Defendants' LCDs and LCD products to customers and users in the United States.

COUNT I
INFRINGEMENT OF THE '002 PATENT

35. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

36. Defendants have infringed, and/or induced infringement of the '002 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that infringes one or more claims of the '002 Patent in this judicial district and elsewhere in the United States.

37. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '002 Patent, either literally or equivalently.

38. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '002 Patent and is without adequate remedy at law.

39. Defendants have, upon information and belief, infringed and are infringing the '002 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT II
INFRINGEMENT OF THE '449 PATENT

40. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

41. Defendants have infringed and/or induced infringement of the '449 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that are made by a method that infringes one or more claims of the '449 Patent in this judicial district and elsewhere in the United States.

42. The products made by the infringing method that are used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '449 Patent, either literally or equivalently.

43. LG.Philips has been and will continue to be injured by Defendants' past and continuing infringement of the '449 Patent and is without adequate remedy at law.

44. Defendants have, upon information and belief, infringed and are infringing the '449 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct is lawful. Defendants' infringement has been and continues to be willful and deliberate, and will continue unless enjoined by this Court, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT III
INFRINGEMENT OF THE '737 PATENT

45. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

46. Defendants have infringed and/or induced infringement of the '737 Patent by making, using, causing to be used, offering to sell, causing to be offered for sale, selling, causing to be sold, importing, and/or causing to be imported products that were made by a method that infringed one or more claims of the '737 Patent in this judicial district and elsewhere in the United States.

47. The products made by the infringed method that were used, caused to be used, sold, caused to be sold, offered for sale, caused to be offered for sale, imported, and/or caused to be imported by Defendants meet each and every limitation of at least one claim of the '737 Patent, either literally or equivalently.

48. LG.Philips has been injured by Defendants' infringement of the '737 Patent.

49. Defendants have, upon information and belief, infringed the '737 Patent with knowledge of LG.Philips' patent rights and without a reasonable basis for believing their conduct was lawful. Defendants' infringement has been willful and deliberate, making this an exceptional case and entitling LG.Philips to increased damages and reasonable attorneys' fees pursuant to 35 U.S.C. §§ 284 and 285.

COUNT IV
CLAIM FOR DECLARATORY JUDGMENT OF INVALIDITY OF THE '786 PATENT, THE '923 PATENT, THE '352 PATENT, AND THE '926 PATENT AGAINST DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION

50. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

51. CMO has accused LG.Philips of infringing CMO's United States Patent No. 6,008,786 (the "'786 Patent")(a copy of which is attached as Exhibit D), United States Patent No. 6,013,923 (the "'923 Patent")(a copy of which is attached as Exhibit E), United States Patent No. 5,619,352 (the "'352 Patent")(a copy of which is attached as Exhibit F), and United States Patent No. 6,734,926 B2 (the "'629 Patent")(a copy of which is attached as Exhibit G) by filing a complaint in the U.S. District Court for the Eastern District of Texas. As such, there is a substantial controversy between the parties having adverse legal interests.

52. Claims of the '786 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

53. Claims of the '923 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

54. Claims of the '352 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

55. Claims of the '926 Patent are invalid for failure to satisfy one or more of the requirements for patentability set forth in Title 35 of the United States Code.

56. Because Chi Mei has asserted the Chi Mei Patents against LG.Philips, thereby creating an actual controversy, declaratory relief is both appropriate and necessary to establish that one or more of the claims of the '786 Patent, the '923 Patent, '352 Patent, and the '926 Patent are invalid.

COUNT V
CLAIM FOR DECLARATORY JUDGMENT OF NON-INFRINGEMENT OF THE '786 PATENT, THE '923 PATENT, THE '352 PATENT, AND THE '926 PATENT AGAINST DEFENDANT CHI MEI OPTOELECTRONICS CORPORATION

57. The allegations in the foregoing paragraphs of this Complaint are incorporated by reference herein as if restated and set forth in full.

58. LG.Philips' LCD modules do not infringe any claim of the '786 Patent, either directly or under the doctrine of equivalents.

59. LG.Philips' LCD modules and/or methods of driving LCD modules do not infringe any claim of the '923 Patent, either directly or under the doctrine of equivalents.

60. LG.Philips' LCD modules and/or methods for forming LCD modules do not infringe any claim of the '352 Patent, either directly or under the doctrine of equivalents.

61. LG.Philips' LCD modules and/or methods for forming LCD modules do not infringe any claim of the '926 Patent, either directly or under the doctrine of equivalents.

62. Because Chi Mei maintains that LG.Philips infringes the Chi Mei Patents, thereby creating an actual controversy, a declaration of rights between LG.Philips and Chi Mei is both appropriate and necessary to establish that LG.Philips has not infringed and does not infringe any claim of the '786 Patent, the '923 Patent, '352 Patent, and the '926 Patent.

PRAYER FOR RELIEF

WHEREFORE, Plaintiff LG.Philips prays for judgment as follows:

A. That Chi Mei, Chi Mei USA, AUO, AUO America, Tatung, Tatung America, and ViewSonic have infringed the Patents-in-Suit;

B. That Chi Mei's, Chi Mei USA's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit has been willful;

C. That Chi Mei, Chi Mei USA, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them, are enjoined and restrained from continued infringement, including but not limited to using, making, importing, offering for sale and/or selling products that infringe, and from inducing the infringement of, the '002 Patent and '449 Patent, prior to their expiration, including any extensions;

D. That Chi Mei, Chi Mei USA, AUO, AUO America, Tatung, Tatung America, and ViewSonic and their parents, subsidiaries, affiliates, successors, predecessors, assigns, and the officers, directors, agents, servants and employees of each of the foregoing, and those persons acting in concert or participation with any of them deliver to LG.Philips all products that infringe the Patents-in-Suit for destruction at LG.Philips' option;

E. That a judgment be entered against Chi Mei declaring that the claims of United States Patent No. 6,008,786, United States Patent No. 6,013,923, United States Patent No. 5,619,352, and United States Patent No. 6,734,926 B2 are each invalid, and thus unenforceable against LG.Philips, its officers, agents, servants and employees;

F. That a judgment be entered against Chi Mei declaring that LG.Philips has not infringed and does not infringe any claim of United States Patent No. 6,008,786, United States Patent No. 6,013,923, United States Patent No. 5,619,352, and United States Patent No. 6,734,926 B2;

G. That LG.Philips be awarded monetary relief adequate to compensate LG.Philips for Chi Mei's, Chi Mei USA's, AUO's, AUO America's, Tatung's, Tatung America's, and

ViewSonic's acts of infringement of the Patents-in-Suit within the United States prior to the expiration of the Patents-in-Suit, including any extensions;

H. That any monetary relief awarded to LG.Philips regarding the infringement of the Patents-in-Suit by Defendants be trebled due to the willful nature of Chi Mei's, Chi Mei USA's, AUO's, AUO America's, Tatung's, Tatung America's, and ViewSonic's infringement of the Patents-in-Suit;

I. That any monetary relief awarded to LG.Philips be awarded with prejudgment interest;

J. That this is an exceptional case and that LG.Philips be awarded the attorneys' fees, costs and expenses that it incurs prosecuting this action; and

K. That LG.Philips be awarded such other and further relief as this Court deems just and proper.

JURY DEMAND

Plaintiff demands a trial by jury of any and all issues triable of right by a jury.

THE BAYARD FIRM

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May 22, 2007

EXHIBIT A

United States Patent [19]

Holmberg

[11] **Patent Number: 5,019,002**

[45] **Date of Patent: May 28, 1991**

[54] **METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY**

[75] Inventor: **Scott H. Holmberg**, San Ramon, Calif.

[73] Assignee: **Honeywell, Inc.**, Minneapolis, Minn.

[21] Appl. No.: **218,312**

[22] Filed: **Jul. 12, 1988**

[51] **Int. Cl.**[5] **H01L 45/00**

[52] **U.S. Cl.** **445/24**; 357/23.13; 437/56

[58] **Field of Search** 445/24, 3; 357/23.13, 357/4; 437/4, 8, 56

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,455,739	6/1984	Hynecek	427/8 X
4,586,242	5/1986	Harrison	437/8
4,714,949	12/1987	Simmons et al.	357/23.13
4,736,271	4/1988	Mack et al.	357/23.13
4,803,536	2/1989	Tuan	357/23.13

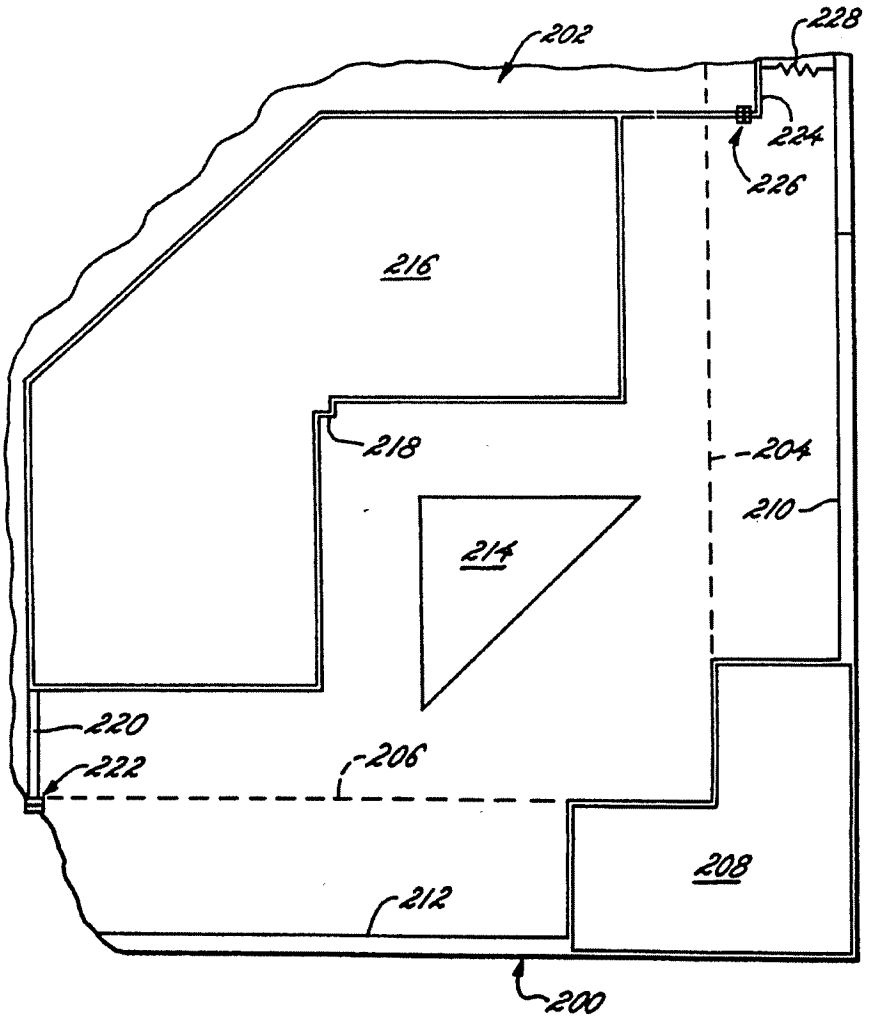
Primary Examiner—Kenneth J. Ramsey

Attorney, Agent, or Firm—Leydig, Voit & Mayer

[57] **ABSTRACT**

Flat panel displays are provided including protection from electrostatic discharge (ESD) during manufacture and thereafter. At least one ESD guard ring is provided to protect the active elements of the display from the potential discharge between the row and column lines. An internal ESD guard ring is coupled to the row and column lines via shunt transistors. An external ESD guard ring is coupled to the row and column lines via a resistance. Both of the guard rings can be provided; however, the external guard ring is removed prior to completion of the display.

36 Claims, 5 Drawing Sheets



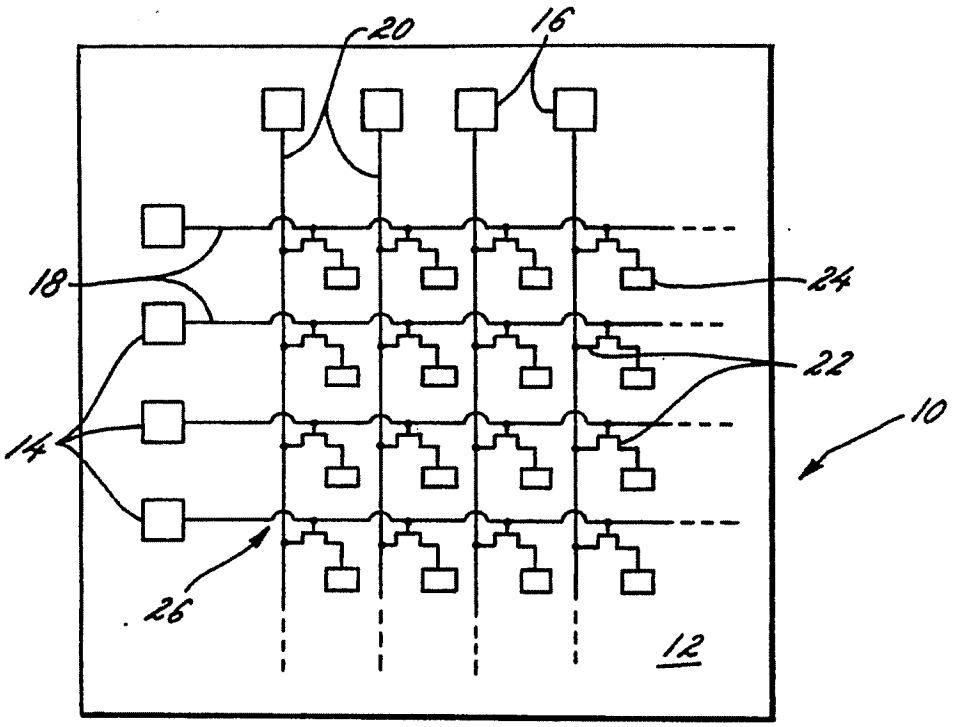


FIG. 1

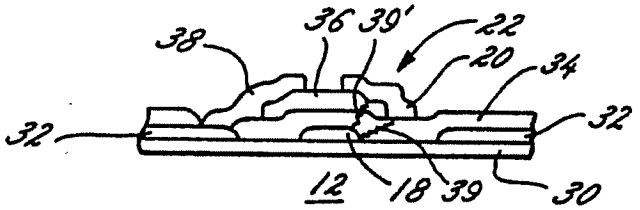


FIG. 2

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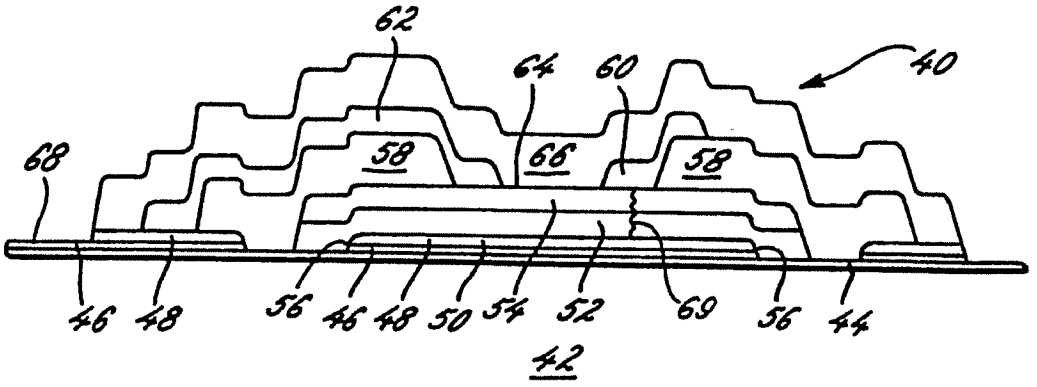


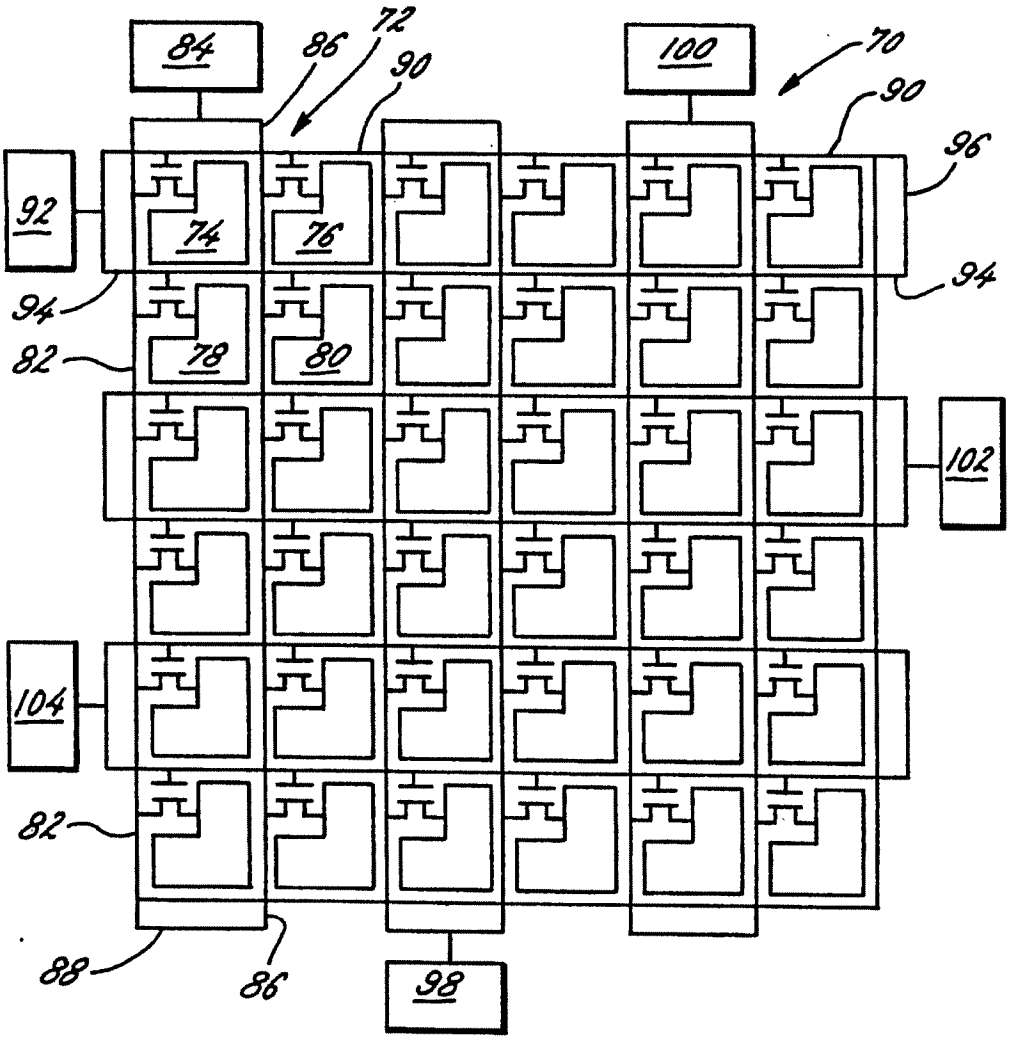
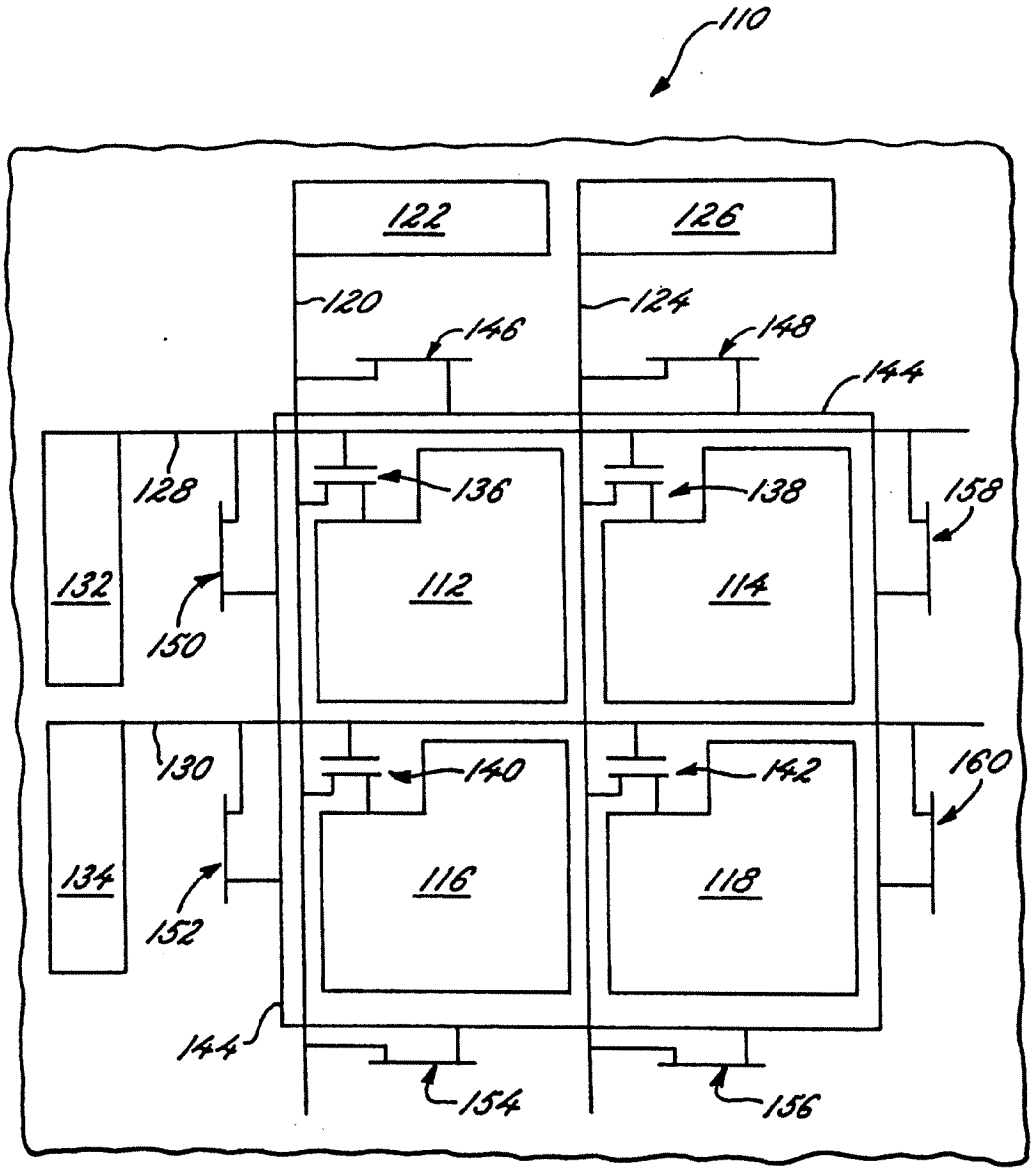


FIG. 4

FIG. 5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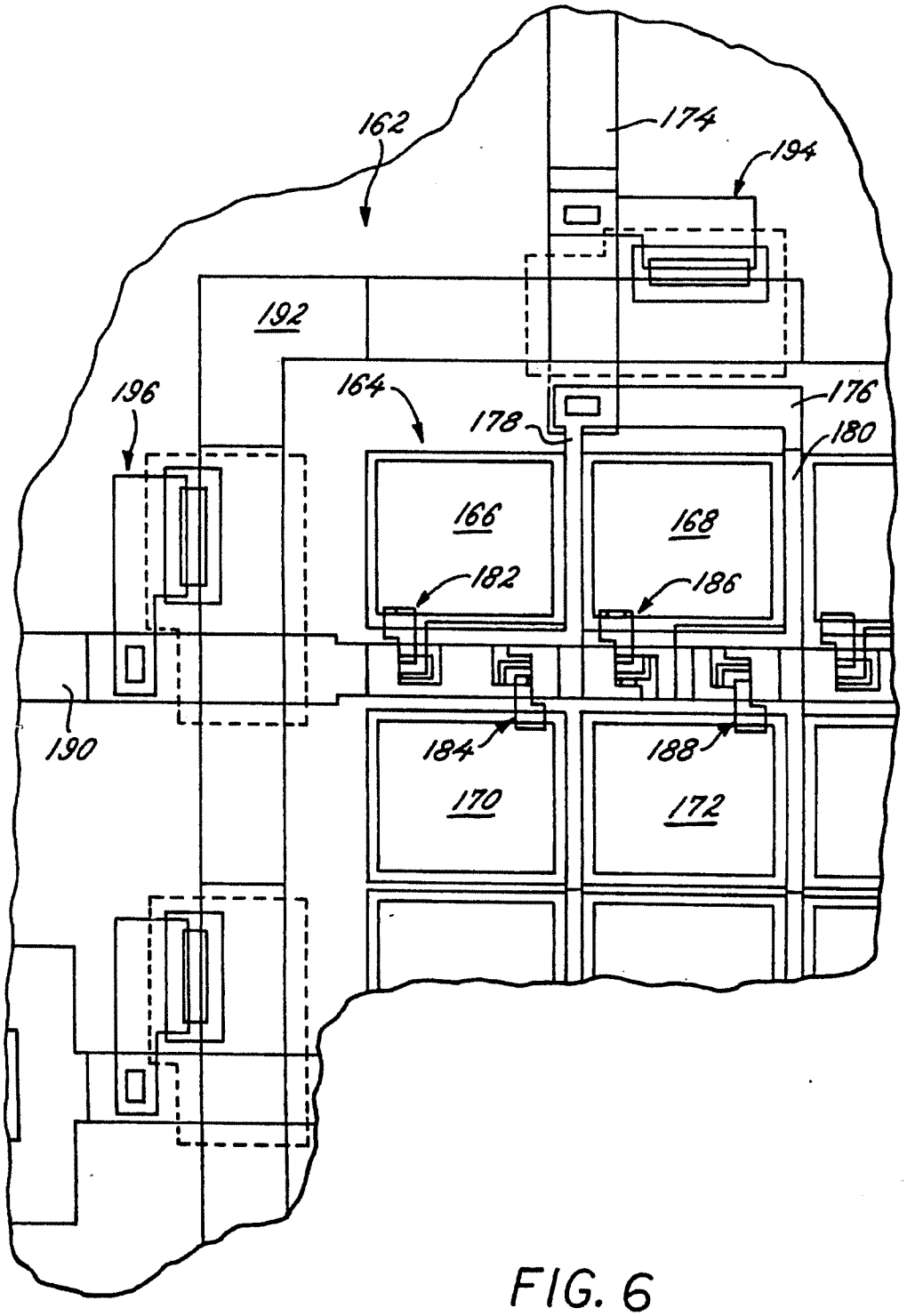
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FIG. 6

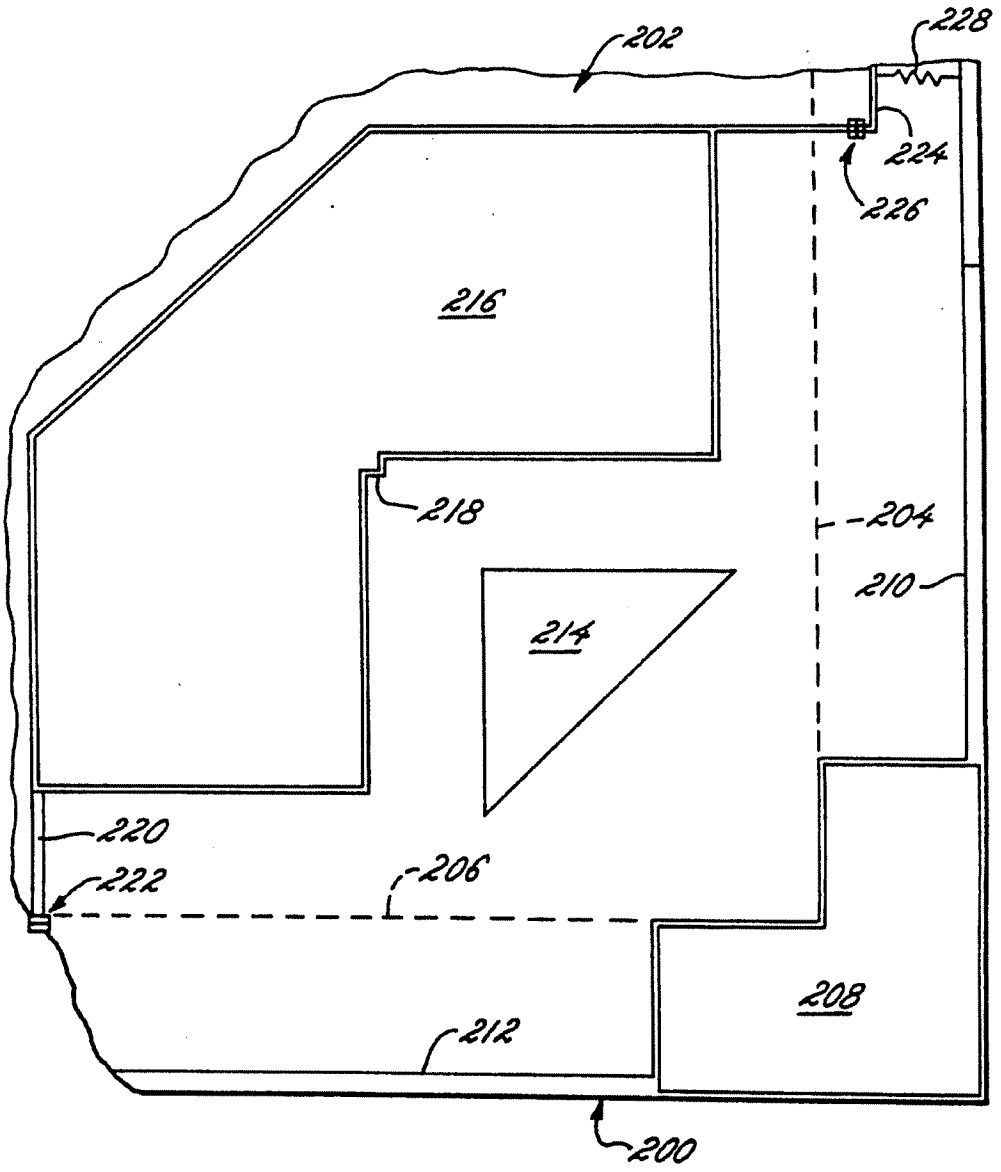

FIG. 7

METHOD OF MANUFACTURING FLAT PANEL BACKPLANES INCLUDING ELECTROSTATIC DISCHARGE PREVENTION AND DISPLAYS MADE THEREBY

BACKGROUND OF THE INVENTION

The present invention pertains to improved flat panel displays and methods of making the displays with protection from electrostatic discharges. More particularly, the present invention is directed to methods of increasing the manufacturing yields of flat panel display backplanes and the displays made therefrom by improving handling characteristics.

In recent years there has been growing interest in flat panel displays, such as those which employ liquid crystals, electrochromic or electroluminescence, as replacements for conventional cathode ray tubes (CRT). The flat panel displays promise lighter weight, less bulk and substantially lower power consumption than CRT's. Also, as a consequence of their mode of operation, CRT's nearly always suffer from some distortion. The CRT functions by projecting an electron beam onto a phosphor-coated screen. The beam will cause the spot on which it is focused to glow with an intensity proportional to the intensity of the beam. The display is created by the constantly moving beam causing different spots on the screen to glow with different intensities. Because the electron beam travels a further distance from its stationary source to the edge of the screen than it does to the middle, the beam strikes various points on the screen at different angles with resulting variation in spot size and shape (i.e. distortion).

Flat panel displays are manufactured to be substantially free of such distortion. In the manufacture of flat panel displays the circuit elements are deposited and patterned, generally by photolithography, on a substrate, such as glass. The elements are deposited and etched in stages to build a device having a matrix of perpendicular rows and columns of circuit control lines with a pixel contact and control element between the control line rows and columns. The pixel contact has a medium thereon which is a substance that either glows (active) or changes its response to ambient light (passive) when a threshold voltage is applied across the medium control element. The medium can be a liquid crystal, electroluminescent or electrochromic materials such as zinc sulfide, a gas plasma of, for example, neon and argon, a dichroic dye, or such other appropriate material or device as will luminesce or otherwise change optical properties in response to the application of voltage thereto. Light is generated or other optical changes occur in the medium in response to the proper voltage applied thereto. Each optically active medium is generally referred to as a picture element or "pixel".

The circuitry for a flat panel display is generally designed such that the flat panel timeshares, or multiplexes, digital circuits to feed signals to one row and column control line of the pixels at a time. Generally one driving circuit is used for each row or column control line. In this way a subthreshold voltage can be fed to an entire row containing hundreds of thousands of pixels, keeping them all dark or inactive. Then a small additional voltage can be supplied selectively to particular columns to cause selected pixels to light up or change optical properties. The pixels can be made to glow brighter by applying a larger voltage or current of a longer pulse of voltage or current. Utilizing liquid crystal displays (LCD's) with twisted nematic active material, the display is substantially transparent when not activated and becomes light absorbing when activated. Thus, the image is created on the display by sequentially activating the pixels, row by row, across the display. The geometric distortion described above with respect to CRT's is not a factor in flat panel displays since each pixel sees essentially the same voltage or current.

One of the major problems that arises with respect to the prior art method of manufacture of backplanes for active matrix displays (e.g. those employing thin film transistors at each pixel) is that they generally suffer production yield problems similar to those of integrated circuits. That is, the yields of backplanes produced are generally not 100% and the yield (percentage of backplanes with no defects) can be 0% in a worst case. High quality displays will not tolerate any defective pixel transistors or other components. Also, larger size displays are generally more desirable than smaller size displays. Thus, a manufacturer is faced with the dilemma of preferring to manufacture larger displays, but having to discard the entire product if even one pixel is defective. In other words, the manufacturer suffers a radically increased manufacturing cost per unit resulting from decreasing usable product yield.

One solution to the low yield problem is disclosed in U.S. Ser. No. 948,224, filed Dec. 31, 1986, now U.S. Pat. No. 4,676,761 entitled "Method of Manufacturing Flat Panel Backplanes Including Improved Testing and Yields Thereof and Displays Made Thereby", which is owned by the assignee of the present application and is incorporated herein by reference.

These problems of increased cost and decreased yield are improved in the present invention by providing methods of manufacturing display backplanes and the resulting displays with electrostatic discharge protection which provide protection against fatal defects during and after manufacture of the displays.

SUMMARY OF THE INVENTION

There is provided improved methods of manufacturing backplanes and the resulting flat panel displays to increase the manufacturing yield, decrease manufacturing costs and substantially eliminate fatal display defects caused by electrostatic discharge during manufacture and thereafter.

These improvements are accomplished by forming at least one electrostatic discharge (ESD) guard ring around the active elements of the display. An internal ESD guard ring can be formed, which provides a discharge path for static potential applied across the row and column line of the display. This prevents the potential from discharging between the row and column lines through an active element causing a short and resulting in a defect in the display during manufacture or thereafter. An external ESD guard ring can be formed, which provides protection during manufacture of the displays, however, the external ESD guard ring is removed at the end of the display manufacturing process. The displays also can include both the internal and external ESD guard ring to provide protection during manufacture and thereafter.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a plan view schematic representation of an active matrix display backplane made by a prior art method;

FIG. **2** is a cross-section of one transistor of the prior art backplane which could be utilized with the present invention;

FIG. **3** is a cross-section of one transistor which could be utilized with the present invention;

FIG. **4** is a plan view schematic representation of one prior embodiment of a subpixel matrix display;

FIG. **5** is a plan view schematic representation of a matrix display illustrating one embodiment of an internal ESD guard ring of the present invention;

FIG. **6** is an enlarged plan view of a portion of one embodiment of a subpixel matrix display illustrating the internal ESD guard ring in accordance with the present invention; and

FIG. **7** is a partial plan view of one embodiment of an exterior ESD guard ring of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now more particularly to FIG. **1**, there is shown a schematic representation of an active matrix flat panel display device **10** made in accordance with conventional photolithographic techniques. One such device **10** and the manufacture thereof is more fully described in Application of Amorphous Silicon Field Effect Transistors in Addressable Liquid Crystal Display Panels, A. J. Snell, et al., *Applied Physics,* No. 24, p. 357, 1981. The device **10** includes a substrate **12**, sets of contact pads **14** and **16**, sets of control or bus lines **18** and **20**, and, in this particular example of the prior art, transistors **22** and pixel back contacts **24**.

The substrate **12** commonly employed in these devices is formed from glass. The control lines **18** and **20** are organized into a matrix of rows **18** and columns **20**. The control line rows **18** in this device **10** serve as gate electrodes and the control line columns **20** as source connections. One contact pad **14** is connected to one end of each of the row control lines **18**. One contact pad **16** is connected to one end of each of the column control lines **20**. The display drive control (not shown) is connected to the sets of pads **14** and **16**.

At each matrix crossover point **26**, where a row line **18** and a column line **20** cross, a switching element, transistor **22** is formed to connect the row line **18** and column line **20** to the pixel back contacts **24**. The active medium is deposited at least on the contacts **24** which will optically change properties in response to the combined voltages or currents in the respective crossover point **26** formed by the row **18** and column **20**. The active medium at a given crossover point **26** will appear as a square or dot in the overall checkerboard type matrix of the display **10**. The actual size of the transistors **22** and the contacts **24** are not now drawn to scale, but are shown schematically for illustration only.

It should be noted that theoretically there is no limit on the number of rows **18** and columns **20** that can be employed, only a portion of which are illustrated in FIG. **1**. Therefore, there is also no theoretical limit on the outside dimensions of such a device **10**. However, the present state of the lithographic art places a practical limit on the outside dimensions of these devices. The present alignment techniques generally allow high resolution display devices to be manufactured approximately five inches on a side **28**, although improved techniques of up to fourteen inches on a side has been demonstrated.

The problem encountered by the prior art method of manufacture is that if the array of device **10** contains any defective pixel transistors **22** or other circuit elements causing a pixel to be inoperative, it must be discarded.

Referring in detail to FIG. **2**, several problems occur when the switching element, transistor **22** is manufactured. The substrate **12** is a substantial portion of the backplane cost and hence an inexpensive soda-lime glass is generally utilized. It has been demonstrated by liquid crystal display manufacturers that the high sodium concentration can poison the liquid crystal materially diffusing through the overlying ITO layer and hence an SiO_2 suppression layer **30** is generally formed on the substrate **12**. There are some high quality low sodium types of substrates available, which would not need the suppression layer **30**. An ITO layer **32** is formed and etched to provide an ITO free area on which the gate **18** is deposited. Following the deposition of the gate **18**, a gate insulator layer **34** is deposited. Although a smooth uniform coverage of the gate **18** by the insulator **34** is illustrated, in production the gate **18** has or can have sharp edges which lead to pin holes or thinning of the insulator **34** at the gate edges. The source and drain metals can short to the gate **18**. The thinning or pin holes produce transistors **22**, which if operative, do not have uniform operating characteristics and hence the backplane is worthless.

One attempt to solve this problem, is to make the gate **18** very thin, but the resistivity is then too high to make the large arrays necessary for the backplane. A second attempt to solve the problem, is to make the gate insulator **34** very thick, but this decreases the gain of the transistor **22** and is also self defeating.

An amorphous silicon layer **36** is then deposited, with the source **20** and a drain **38** deposited thereover. A passivating layer (not shown) would be deposited over the completed structure to complete the transistor **22**. During operation the activation of the source **20** and the gate **18** couples power through the silicon alloy **36** to the drain and hence to the contact pad **24** formed by the ITO layer **32**.

During manufacture of the device **10**, electrostatic discharge can occur when a high static electric potential is coupled across at least one pair of the gate lines **18** and the source lines **20**. The discharge frequently will result in a short **39** through the insulator **34** or a short **39'** through the insulator **34** and the silicon layer **36** in the transistor **22**, between the adjacent crossover points of the lines **18** and **20** as can be seen in FIG. **2**. This will cause at least one row and one intersecting column of the display pixels to be defective and in the type of display device **10**, generally the defect will be a fatal one (clearly visible) and hence the device will be discarded. The device **10** does not provide any redundancy or subpixels and hence the defect cannot easily be isolated.

Referring now to FIG. **3**, there is shown a schematic representation of one embodiment of a transistor **40** which can be utilized with the present invention. The transistor is more fully disclosed in U.S. Pat. Nos. 4,545,112 and 4,736,229, which are incorporated herein by reference.

A glass substrate **42** includes a barrier SiO_2 layer **44** thereon. As above mentioned, a low sodium glass sub-

strate, such as Corning 7059 glass, could be utilized, and hence the barrier layer **44** can be eliminated. The detailed deposition steps are described in the above-referenced patent and application. An ITO layer **46** is deposited and then a refractory metal layer **48** is deposited on the ITO layer **46**.

The layers **46** and **48** are etched to form a gate electrode **50**. A gate insulator **52** and a semiconductor material **54** are sequentially deposited over the gate **50**. The material **54** preferably is an amorphous silicon alloy. To avoid the possibility of any gate to source or drain shorts at gate edges **56**, a dielectric **58** is deposited over the gate **55**, the gate insulator **52** and the semiconductor **54**. The dielectric **58** is deposited to a sufficient thickness to ensure that no shorts or thin spots are formed between the edges **56** of the gate **50** and a source **60** and a drain **62** deposited thereover.

The dielectric **58** is etched away only on a substantially planar central region **64** of the semiconductor layer **54**. This insures uniform operating characteristics for the transistors **40** in the backplane array. A passivating layer **66** is deposited over the whole structure to complete the structure of the transistor **40**.

During all of the transistor processing steps, the refractory metal layer **48** remains over a pixel contact pad **68** upon which the active material of the pixel is deposited. As a final step, before the active medium (not shown) is added to the backplane to complete the display, the refractory metal is etched off of the pixel pad **68** leaving the ITO layer **46** exposed after all the processing has been completed.

The gate to source or drain shorts referred to above in discussing the dielectric **58**, refer to physical shorts caused by thin spots or actual metal particles or filaments. The electrostatic discharges caused during manufacturing and thereafter will be deterred by the dielectric **58**, but will not be eliminated. The potential can be high enough to again form a short **69** through the gate insulator **52** and the semiconductor material **54** in the transistor **40**, between the source **60** and the gate **50**. Depending upon the display structure, at least one pixel or one subpixel (FIG. **4**) will be defective.

Referring now to FIG. **4**, a subpixel matrix display of the above-referenced application, U.S. Ser. No. 948,224, is designated generally by the reference numeral **70**. The subpixel matrix display **70** is illustrated as having each pixel subdivided into four subpixels, but the pixels could be subdivided into numerous other configurations such as two subpixels, two by four or six subpixels or in three subpixels for color applications. Each pixel **72** is subdivided into four subpixels **74**, **76**, **78** and **30** (only one pixel **72** is so numbered for illustration). As previously stated, the number of pixels is merely shown for illustration purposes and the display **70** could contain any desired number and configuration, square or rectangular.

A column (source) line or bus **82** connects the subpixels **74** and **78** and all other column subpixel pairs in one-half of each of the pixels to a column or source contact pad **84** at one edge of the display **70**. A second column (source) line or bus **86** connects the subpixels **76** and **80** and all other column subpixel pairs in the second half of each of the pixels to the column or source contact pad **84**. The bus lines **82** and **86** are interconnected (shorted) at or before the pad **84** and are interconnected (shorted) at the opposite ends by a line or short **88**.

A row (gate) line or bus **90** connects the subpixels **74** and **76** and all other row subpixel pairs in one-half of each of the pixels to a row (gate) pad **92**. A second row (gate) line or bus **94** connects the subpixels **78** and **80** and all other row subpixel pairs in one-half of each of the pixels to the row pad **92**. The bus lines **90** and **94** are interconnected (shorted) at or before the pad **92** and are interconnected (shorted) at the opposite ends by a line or short **96**.

In a like manner, each of the other subpixel pairs are connected in columns to respective column (source) pads **98** and **100**, etc. The pads **84**, **98** and **100** are illustrated as being an opposite sides of the display to provide additional connecting space for the pads, however, they also could all be on one side as in the display **10**. Each of the other subpixel pairs also are connected in rows to respective row (gate) pads **102** and **104**, etc.

The pixel **72** then is divided into four subpixels **74**, **76**, **78** and **80** which allows for one of the subpixels to be defective, such as the subpixel **74**, without causing a fatal defect, since the remaining three subpixels **76**, **78** and **80** remain operative. In prior devices, the pixel **72** would be totally defective and hence the display **70** would be inoperable.

Further, one often fatal display defect is caused by a defect or open in one of the row or column bus lines which would cause the whole row or column to be out, again resulting in an inoperative display **70**. With the respective subpixels pairs of row and column bus lines interconnected, however, an open in a bus line will at most cause one subpixel to be inoperative. An open in one or more of the bus lines between the subpixels will result in no defects, since the current is supplied from the opposite shorted end of the row or column bus line. Thus, the display **70** in effect has redundant row and column bus lines.

To avoid the fatal defect of the multiple open lines, as also disclosed in U.S. Ser. No. 948,224, the redundant row and column bus lines can be further interconnected at each subpixel. Each pair of the column bus lines **82** and **86** are additionally interconnected between each of the subpixels **74**, **78**, etc. by respective lines or shorts. In a like manner, each pair of the row bus lines **90** and **94** are interconnected between each of the subpixels **74**, **76**, etc. by respective lines or shorts. Further, although both the row bus lines and the column bus lines can be interconnected between each subpixel, only one of the row or the column bus line sets might be shorted to limit the loss of active pixel display area.

The short **69** in one of the active devices in the display **70** can be eliminated by opening the row or column line between the short and the line. This results in only one subpixel, such as the subpixel **74** being defective and due to the small size of the subpixel, is not a fatal defect (i.e. not readily visual). The rest of the corresponding column and row subpixels would be operable due to the redundant and interconnected row and column bus lines.

Referring now to FIG. **5**, a matrix display incorporating one embodiment of an internal ESD guard ring of the present invention is designated generally by the reference numeral **110**. The matrix display **110** is illustrated having four pixels **112**, **114**, **116** and **118**. The pixels, however, can be subdivided into numerous subpixel configurations such as two or four subpixels, two by four or six subpixels or in three subpixels for color display applications. Also, as previously stated for the

subpixel matrix display **70**, the number of pixels can be of any number and configuration, square or rectangular.

A column (source) line or bus **120** connects the pixels **112** and **116** and all other pixels in the same column to a source contact pad **122** at one edge of the display **110**. A source line **124** connects the pixels **114** and **118** to a source contact pad **126**. In a like manner, a pair of row (gate) lines **128** and **130** connect respective pairs of pixels **112**, **114** and **116**, **118** in each row to respective gate pads **132** and **134**.

Each pixel **112**, **114**, **116** and **118** includes a respective active element, such as transistors **136**, **138**, **140** and **142** which couple the pixels to the respective source lines **120** or **124** and gate lines **128** or **130**. To prevent a large electrostatic potential discharging through one of the transistors **136**, **138**, **140** and **142**, an internal ESD guard ring **144** is formed around the pixels **112**, **114**, **116** and **118**. The guard ring **144** is illustrated as a closed ring, but could also be an open L or C-shaped line if the gate and source pads all are on one respective side of the display **110**.

The ESD guard ring **144** also is coupled via respective transistors **146**, **148**, **150** and **152** to, the source and gate lines. The guard ring **144** will be coupled to the end of each source and gate line, so if the source and gate lines include pads at their opposite ends (not illustrated), then the guard ring **144** will include a further respective set of transistors **154**, **156**, **158** and **160**.

The ESD guard ring **144** preferably is formed from a low resistance metal, such as an aluminum alloy. The transistors **146** through **160** can include a floating gate (not illustrated), no gate, or can include an oxide below to form a spark gap.

In operation, with the guard ring **144**, a potential placed upon the source pads **122** will not short one of the transistors **136** or **140**. Instead, the transistor **146** will turn on followed by the transistor **150**, shorting the potential from the pad **122**, via the line **120**, the transistor **146**, the guard ring **144**, the transistor **150** and the line **128** to the pad **132**. Thus, the guard ring **144** will not allow high potentials across the pads **122**, **126**, **132** and **134**. The guard ring **144** preferably is formed concurrently with the display elements and is not removed, providing continuous protection even following manufacture of the display **110**.

A specific subpixel display incorporating an internal guard ring of the invention is best illustrated in FIG. **6** and is designated generally by the reference numeral **162**. The display **162** includes a plurality of pixels, each having four subpixels in a similar fashion to the display **70** illustrated in FIG. **4**. Only one pixel **164** is illustrated in detail and includes four subpixels **166**, **168**, **170** and **172**. A source line **174** includes a shorting line **176** which is connected to a pair of source lines **178** and **180**, coupled to each of the subpixels by a respective transistor structure **182**, **184**, **186** and **188**, which are not described in detail. The transistors **182**, **184**, **186** and **188** also couple the subpixels **166**, **168**, **170** and **172** to a gate line **190**.

An internal ESD guard ring **192** is coupled via a transistor structure **194** to the source line **174** and via a transistor structure **196** to the gate line **190**. The guard ring **192** and transistors **194** and **196** operate as before described to short any potential to ground. The low value of the normal operating voltages does not turn on the transistors **194** and **196**, which do not effect the normal display operation.

The ESD preventive structure can also include an outer ESD guard ring **200**, best illustrated in FIG. **7**. Only one corner portion **202** of the display and guard ring **200** is illustrated. While the display is being manufactured, the outer guard ring **200** is connected to all of one of the source and gate pads (not illustrated), which pads are serially connected together via jumpers outside of scribe lines **204** and **206**. A corner pad **208** is connected to each other corner pad (not illustrated) by respective outer conductive lines **210** and **212** of the guard ring **200**. The L-shaped corner pad **208** can be grounded and also provides the alignment for the scribe lines **204** and **206**, which are utilized to disconnect the source and gate jumpers and the guard ring **200** after the structure is completed. The corner portion **202** includes a triangular pad **214** which provides alignment for diagonal corner displays, when utilized.

A backplane pickup contact pad **216** also is provided, which includes a corner **218** for aligning the backplane with the front plane. The pad **216** includes a shunt line **220** which is connected to one set of source or gate lines via a shunt transistor **222** along the edge to be scribed and removed along the line **206**. The line **210** is connected to the other set of gate or source lines by a shunt line **224**, a shunt transistor **226** and a large resistance **228**, such as 100 K ohms (illustrated schematically). The outer ESD guard ring **200** provides ESD protection only during manufacture of the display and is removed prior to completion of the display. The resistance **228** provides an ESD short for high electrostatic potentials, which can be incurred during manufacturing of the display which can be connected anywhere between the line **210** and the other set of gate or source lines. The resistance **228** minimizes the discharge current surge and the shunt transistors **222** and **226** act as before described. There will be at least one corner backplane pickup pad **216** and preferably there will be two or three, each with their associated shunt transistors.

The outer guard ring lines **210** and **212** preferably are formed at the same time as the firs: of the gate or source lines. The inner guard ring **44** and the associated shunt transistors of both guard rings preferably are formed concurrently with the other display structures. The scribe lines **204** and **206** can be prescribed, but left intact until the back and front planes are mated and then removed to provide the gate and source contacts for the printed circuit board connections.

Modification and variations of the present invention are possible in light of the above teachings. The transistors **22** or other types of two or three terminal switching devices can be utilized with the invention. The amorphous silicon alloy semiconductor material **54**, could be any of numerous types of materials such as CdSe or GaAs materials. The ESD guard rings can be utilized separately or together with all types of active element matrix displays and not just those illustrated. The shunt transistors **146**, **194** and **222**, etc. also can be formed as other active switching elements, such as diodes. It is therefore to be understood that within the scope of the appended claims, the invention may be practiced otherwise than as specifically described.

What is claimed and desired to be secured by Letters Patent of the United States is:

1. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines, interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another;

forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

2. The method as defined in claim **1** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

3. The method as defined in claim **2** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

4. The method as defined in claim **3** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

5. The method as defined in claim **3** including forming a corner on said pad to align the front plane and back plane of the display.

6. The method as defined in claim **3** including forming a plurality of pickup pads, each one on a separate corner of the display.

7. The method as defined in claim **1** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

8. The method as defined in claim **1** including forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

9. The method as defined in claim **8** including forming separate shunt switching elements between said inner guard ring and each row and column line.

10. A method of manufacturing active matrix display backplanes and displays therefrom, comprising:

providing a substrate;

forming a pattern of pixels on said substrate;

forming a plurality of row and column intersecting pixel activation lines; and

forming an inner electrostatic discharge guard ring on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

11. The method as defined in claim **10** including forming separate shunt switching elements between said inner guard ring and each row and column line.

12. The method as defined in claim **10** including interconnecting substantially all of said row lines to one another and substantially all of said column lines to one another and forming an outer electrostatic discharge guard ring on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays; and

removing said outer guard ring and row and column interconnections prior to completion of the display.

13. The method as defined in claim **12** including coupling one plurality of said interconnected row and column lines to said outer guard ring via said resistance.

14. The method as defined in claim **13** including forming at least one pickup pad coupled to said resistance via a shunt switching element.

15. The method as defined in claim **14** including coupling said pickup pad to the other plurality of said interconnected row and column lines via another shunt switching element.

16. The method as defined in claim **14** including forming a corner on said pad to align the front plane and back plane of the display.

17. The method as defined in claim **10** including forming a plurality of pickup pads, each one on a separate corner of the display.

18. The method as defined in claim **10** including forming a corner pad on at least one corner of the display and aligning scribe lines with said corner pad for removing said outer guard ring and row and column intersections.

19. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines, substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another; and

an outer removable electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

20. The backplane as defined in claim **19** including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

21. The backplane as defined in claim **20** including at least one pickup pad coupled to said resistance via a shunt switching element.

22. The backplane as defined in claim **21** including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

23. The backplane as defined in claim **21** including a corner formed on said pad to align the front plane and back plane of the display.

24. The backplane as defined in claim **21** including a plurality of pickup pads, each one formed on a separate corner of the display.

25. The backplane as defined in claim **19** including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

26. The backplane as defined in claim **19** including an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

27. The backplane as defined in claim **26** including separate shunt switching elements formed between said inner guard ring and each row and column line.

28. An active matrix display backplane, comprising:

a substrate;

a pattern of pixels formed on said substrate;

a plurality of row and column intersecting pixel activation lines; and

an inner electrostatic discharge guard ring formed on said substrate coupled to said row and column lines via shunt switching elements to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays and thereafter.

29. The backplane as defined in claim 28 including separate shunt switching elements formed between said inner guard ring and each row and column line.

30. The backplane as defined in claim 28 including substantially all of said row lines interconnected to one another and substantially all of said column lines interconnected to one another and an outer electrostatic discharge guard ring formed on said substrate coupled to said interconnected row and column lines via a resistance to provide protection from electrostatic discharges between said row and column activation lines during manufacture of the displays.

31. The backplane as defined in claim 30 including one plurality of said interconnected row and column lines coupled to said outer guard ring via said resistance.

32. The backplane as defined in claim 31 including at least one pickup pad coupled to said resistance via a shunt switching element.

33. The backplane as defined in claim 32 including said pickup pad coupled to the other plurality of said interconnected row and column lines via another shunt switching element.

34. The backplane as defined in claim 32 including a corner formed on said pad to align the front plane and back plane of the display.

35. The backplane as defined in claim 28 including a plurality of pickup pads, each one formed on a separate corner of the display.

36. The backplane as defined in claim 28 including a corner pad formed on at least one corner of the display and having scribe lines aligned with said corner pad for removing said outer guard ring and row and column intersections.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 5,019,002

DATED : May 28, 1991

INVENTOR(S) : Scott H. Holmberg

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Col. 2, lines 30-31, change "4,676,761" to --4,820,222--;

Col. 4, line 15, change "materially" to --material by--;

Col. 5, line 53, change "30" to --80--;
line 59, change "aIl" to --all--;

Col. 7, line 23, delete the third comma;

Col. 8, line 41, change "firs:" to --first--.

Signed and Sealed this

Twenty-third Day of February, 1993

Attest:

STEPHEN G. KUNIN

Attesting Officer

Acting Commissioner of Patents and Trademarks

EXHIBIT B

US005825449A

United States Patent [19]

Shin

[11] Patent Number: 5,825,449

[45] Date of Patent: Oct. 20, 1998

[54] **LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME**

[75] Inventor: **Woo Sup Shin**, Kyungsangbuk-do, Rep. of Korea

[73] Assignee: **LG Electronics, Inc.**, Seoul, Rep. of Korea

[21] Appl. No.: **781,188**

[22] Filed: **Jan. 10, 1997**

Related U.S. Application Data

[62] Division of Ser. No. 616,291, Mar. 15, 1996.

[30] **Foreign Application Priority Data**

Aug. 19, 1995 [KR] Rep. of Korea 25538/1995

[51] **Int. Cl.**[6] **G02F 1/136**; G02F 1/1343; G02F 1/1345

[52] **U.S. Cl.** **349/148**; 349/149; 349/43

[58] **Field of Search** 349/149, 148, 349/43, 139, 152, 147

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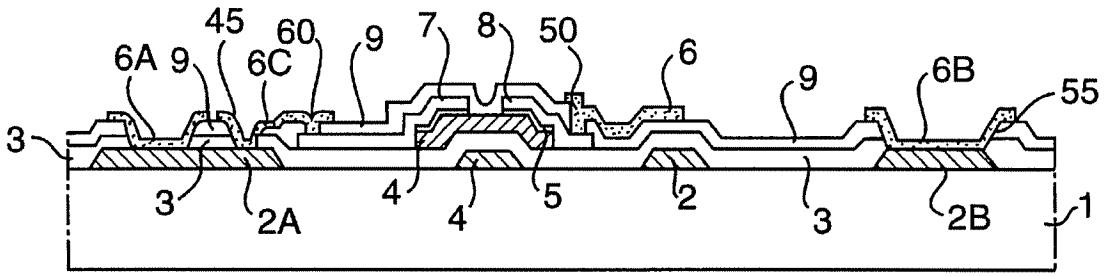
Primary Examiner—William L. Sikes
Assistant Examiner—Tiep H. Nguyen
Attorney, Agent, or Firm—Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P.

[57] **ABSTRACT**

A method for fabricating a liquid crystal display is disclosed whereby a source and gate are exposed after the step of forming a passivation layer. As a result, the number of processing steps is reduced and yield is improved.

11 Claims, 5 Drawing Sheets



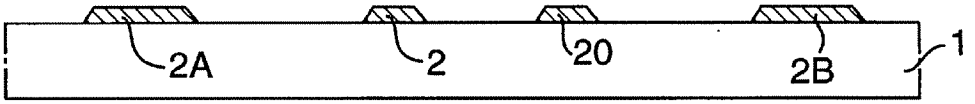


FIG. 1a
PRIOR ART

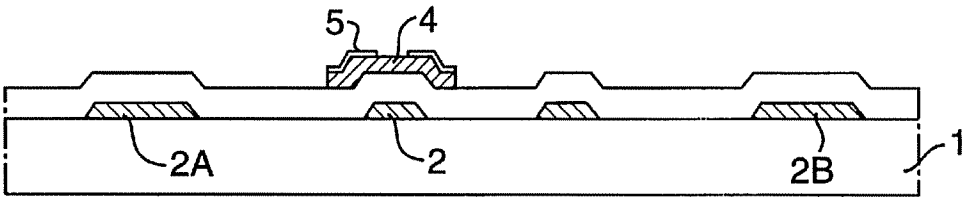


FIG. 1b
PRIOR ART

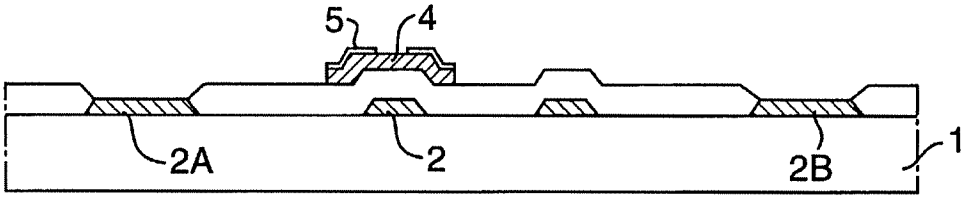


FIG. 1c
PRIOR ART

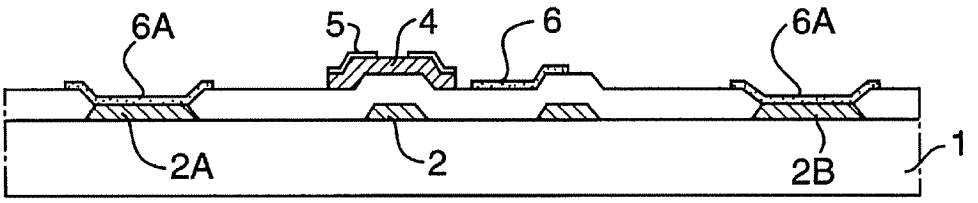


FIG. 1d
PRIOR ART

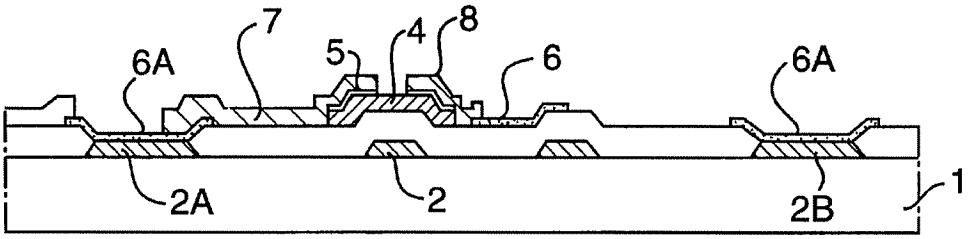


FIG. 1e
PRIOR ART

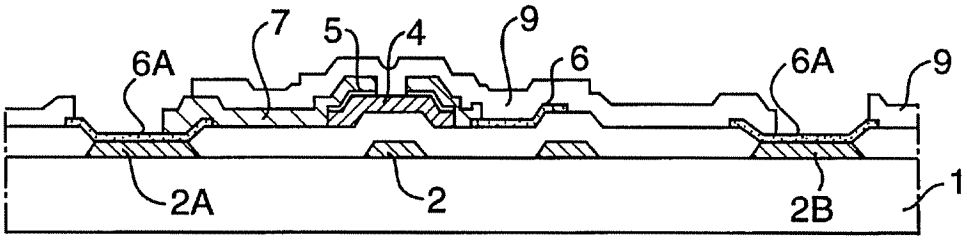


FIG. 1f
PRIOR ART

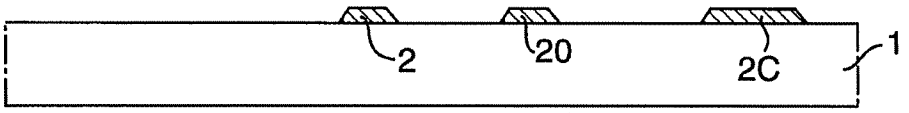


FIG. 2a

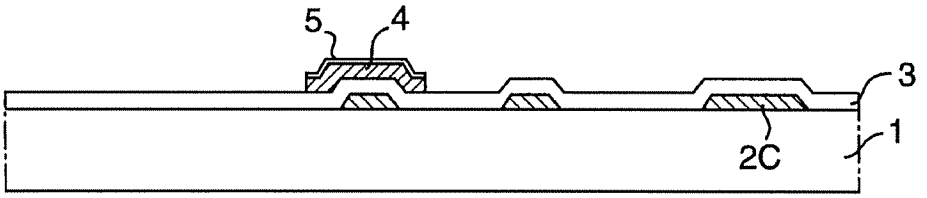


FIG. 2b

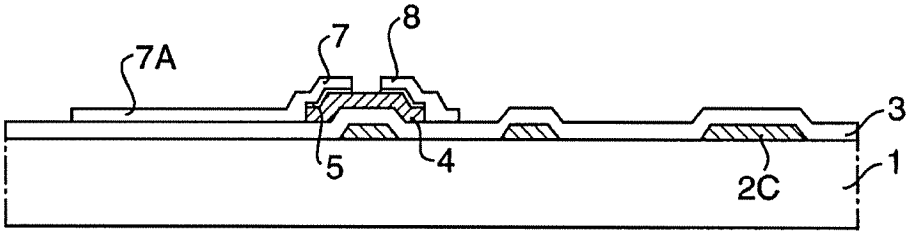


FIG. 2c

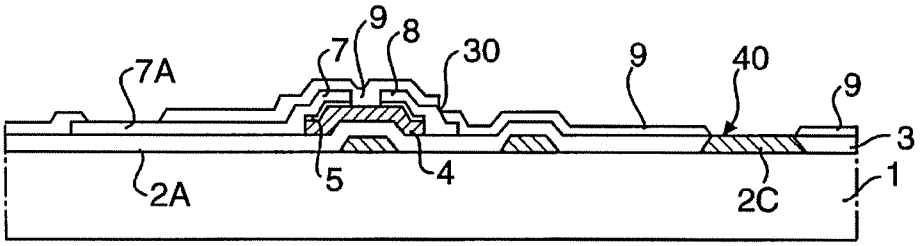


FIG. 2d

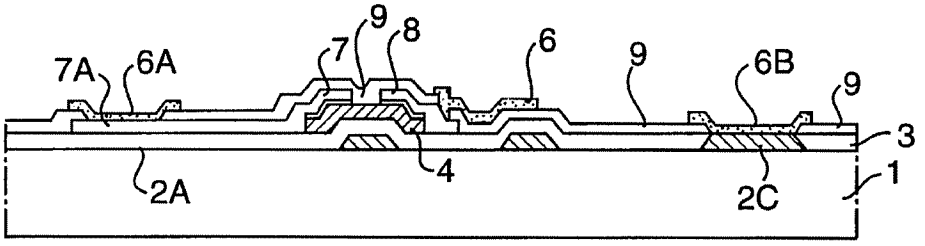


FIG. 2e

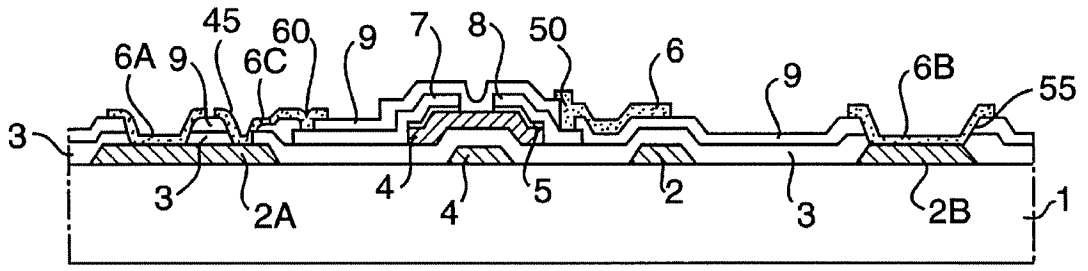


FIG. 3

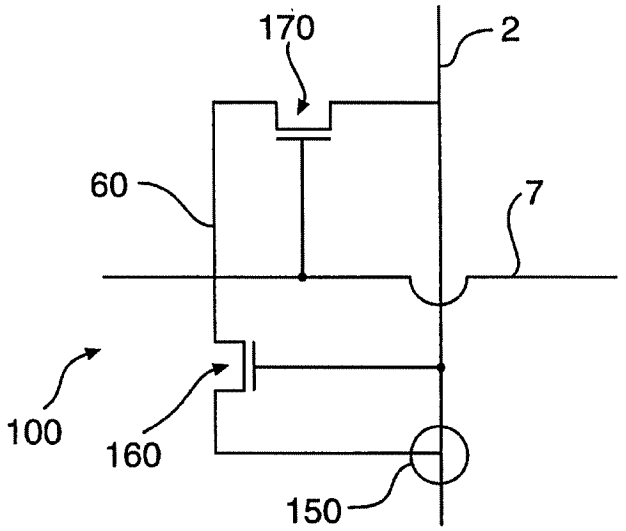


FIG. 4

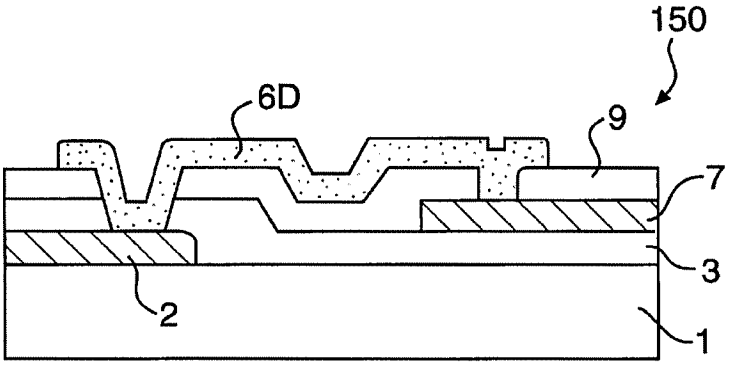


FIG. 5

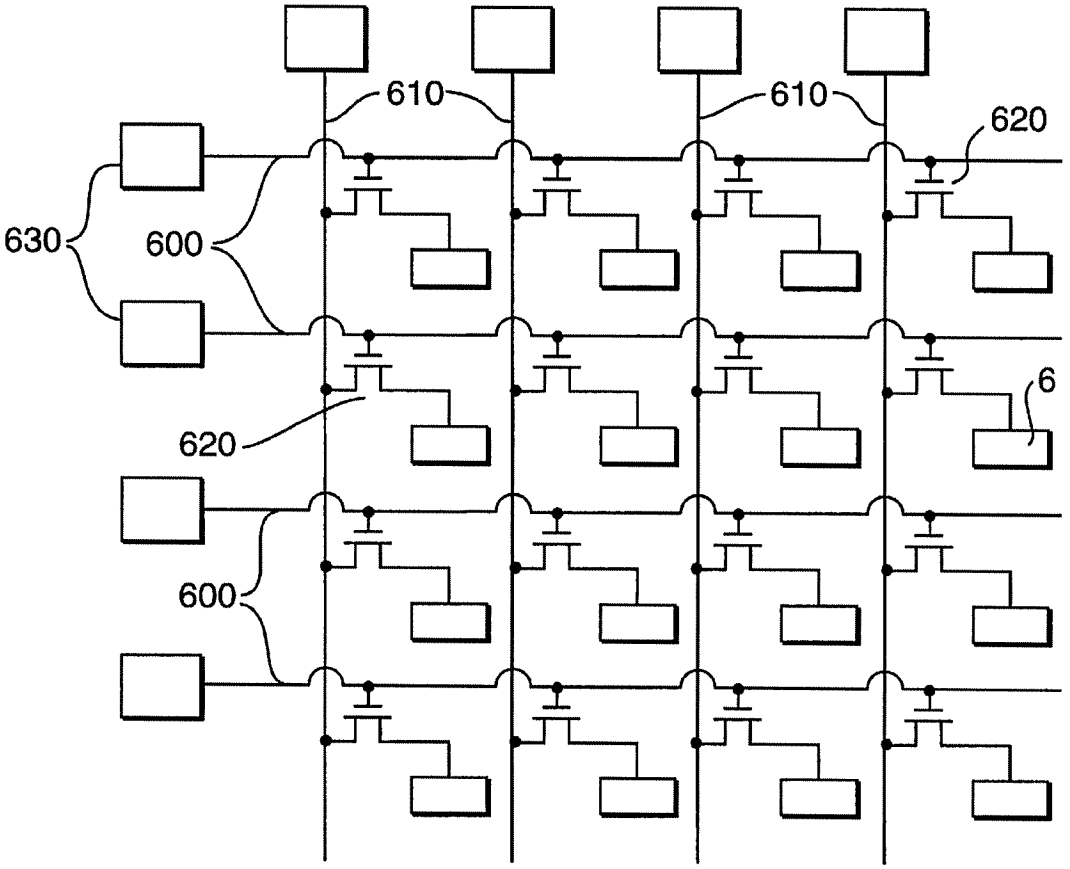


FIG. 6
PRIOR ART

LIQUID CRYSTAL DISPLAY DEVICE AND METHOD OF MANUFACTURING THE SAME

This is a continuation of application Ser. No. 08/616,291, Filed Mar. 15, 1996.

BACKGROUND OF THE INVENTION

The present invention relates to a liquid crystal display (LCD) device and a method of manufacturing the same, and more particularly, to a liquid crystal display device having a combined source electrode and source pad structure.

Active matrix thin film displays include thin film transistors (TFTs) for driving the liquid crystal material in individual pixels of the display. As shown in FIG. **6**, a conventional LCD includes an array of pixels each having liquid crystal material (not shown) sandwiched between a common electrode provided on a top plate (not shown) and a pixel electrode **6** disposed on a bottom plate. The bottom plate further includes a plurality of gate lines **600** intersecting a plurality of data lines **610**.

Thin film transistors **620**, serving as active devices, are located at intersecting portions of gate lines **600** and data lines **610**. Gate lines **600** and data lines **610** are connected to the gates and sources, respectively of thin film transistors **620**. In addition, pixel electrodes **6** are connected to respective drain electrodes of thin film transistors **620**. Gate Pads **630** and Data Pads **640** are connected to the gate lines and data lines to receive datas from gate driver and data driver respectively.

A conventional method of manufacturing a liquid crystal display device including TFT driving elements will be described with reference to FIGS. **1***a*–**1***f*.

As shown in FIG. **1***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, storage capacitor electrode **2**D, source pad **2**A, and gate pad **2**B. Gate pad **2**B is used for receiving a voltage to drive and active layer in the completed TFT device.

As shown in FIG. **1***b*, a gate insulating film **3**, such as a nitride film or an oxide film, is formed on the entire surface of the substrate in order to electrically insulate gate **2**. An amorphous silicon active layer **4** is formed on a portion of gate insulating film **3** overlying gate **2**. Then, in order to reduce the contact resistance between the active layer and the source/drain regions in the completed device, and appropriately doped semiconductor layer **5** is formed on amorphous silicon layer **4** as an ohmic contact layer. Doped semiconductor layer **5** and amorphous silicon layer **4** are then etched in accordance with a predetermined active layer pattern.

Since a pad wiring layer is necessary in order to communicate information from an external driving circuit to the gate and source, a gate insulating film **3** is selectively etched to expose source pad **2**A and gate pad **2**B (see FIG. **1***c*). Next, as shown in FIG. **1***d*, a transparent conductive layer (ITO) is deposited on the entire surface of the substrate and patterned to form a pixel electrode **6**, which is formed on a portion of the display pixel, while ITO patterns **6**A and **6**B are formed on source pad **2**A and gate pad **2**B, respectively.

As shown in FIG. **1***e*, the TFT is formed on the active layer and includes a conductive layer deposited on the substrate and simultaneously patterned to form source and drain electrodes **7** and **8**, respectively. Source electrode **7** is connected to source pad **2**A, and drain electrode **8** is contact with impurity-doped semiconductor layer **5** and pixel electrode **6**. In the completed device structure, source electrode

7 conducts a data signal, received from a data wiring layer and drain electrode **8**, to pixel electrode **6**. The signal is stored in the form of charge on pixel electrode **6**, thereby driving the liquid crystal.

As shown in FIG. **1***f*, a nitride film is deposited on the entire surface of the substrate as a passivation layer **9** in order to seal the underlying device from moisture and to prevent absorption of impurities. Passivation layer **9** is selectively etched to expose source-pad **2**A and gate pad **2**B, thereby completing the TFT.

In the conventional method described above, The source electrode **7** and pixel electrode **6** provided on the same surface of gate insulating film **3**. Accordingly, processing errors can cause these electrodes to contact each other. As a result, shorts can occur, thereby reducing yields.

Further, since the source pad for the source wiring is composed of the same material as the gate, its contact resistance with the underlying source electrode can be high. In addition, at least six masking steps are required as follows: patterning the gate, storage capacitor electrode, source pad and gate pad; forming the active layer pattern; patterning the gate insulating film for exposing the pad part; forming the pixel electrode; forming the source and drain electrode; and patterning the passivation film for exposing the pad part. Thus, the conventional process requires an excessive number of fabrication steps which increase cost and further reduce yield.

SUMMARY OF THE INVENTION

In order to solve the aforementioned problems, it is an objective of the present invention to provide a liquid crystal display device and a method of manufacturing the same, in which processing errors can be prevented and the Yield can be increased by etching the gate insulating film after the step of forming the passivation layer.

To accomplish this objective of the present invention, there is provided a liquid crystal display device comprising a substrate; a gate electrode; a gate pad and a source pad formed on the substrate as a first conductive layer; a gate insulating film formed on the entire surface of the substrate; a semiconductor layer and an impurity-doped semiconductor layer formed on the gate insulating film above the gate electrode; a source electrode and a drain electrode formed on the semiconductor layer; a passivation layer formed on the entire surface of the substrate; a first contact hole exposing the source pad; a second contact hole exposing a portion of the drain electrode; a third contact hole exposing the gate pad portion; and a fourth contact hole exposing the source electrode, the contact holes being formed by etching the passivation layer and gate insulating film; a pixel electrode connected with the drain electrode through the second contact hole; and a transparent conductive layer connecting the source pad with the source electrode through the first contact hole and fourth contact hole.

To further accomplish the objective of the present invention, there is also provided a method of manufacturing a liquid crystal display device, comprising the steps of forming a first conductive layer on a substrate; patterning the first conductive layer to respectively form a gate electrode, a gate pad and a source pad; sequentially forming an insulating film, a semiconductor layer and an impurity-doped semiconductor layer on the entire surface of the substrate; patterning the impurity-doped semiconductor layer and semiconductor layer to an active pattern; forming a second conductive layer on the entire surface of the substrate; patterning the second conductive layer to form a

source electrode and a drain electrode; forming a passivation film on the entire surface of the substrate; Selectively etching the passivation film and insulting film to respectively form a first contact hole exposing the source pad, a second contact hole exposing a portion of the drain electrode, a third contact hole exposing a gate pad portion, and a fourth contact hole exposing a portion of the source electrode; forming a transparent conductive layer on the entire surface of the substrate; and patterning a pixel electrode connected with the drain electrode through the second contact hole, a transparent conductive layer connected with the gate pad through the third contact hole, and a transparent conductive layer connecting the source pad with the source electrode through the first and fourth contact holes.

BRIEF DESCRIPTION OF THE ATTACHED DRAWINGS

FIG. **1***a* to if are cross-sectional views illustrating steps of a conventional method for manufacturing a liquid crystal display device;

FIGS. **2***a* to **2***e* are cross-sectional views illustrating steps of a method for manufacturing a liquid crystal display according to a preferred embodiment of the present invention;

FIG. **3** is a cross-sectional view illustrating a liquid crystal display device structure according to a second embodiment of the present invention;

FIG. **4** is a circuit diagram of one example of a liquid crystal display device in which a gate material is connected with a source material in accordance with a third embodiment of the present invention; and

FIG. **5** is a vertical-cross-sectional view of the device shown in FIG. **4**.

FIG. **6** is a plan view schemetic representation of one prior embodiment of a matrix display.

DETAILED DESCRIPTION OF THE INVENTION

Hereinafter, preferred embodiments of the present invention will be described with reference to the attached drawings.

Referring first to FIG. **2***a*, a conductive layer is formed on a transparent glass substrate **1** and patterned to form a gate electrode **2**, a storage capacitor electrode **2**D, and a gate pad **2**C, all of the same material. The gate electrode is used for applying a voltage in order to drive the active layer in the completed TFT device.

As shown in FIG. **2***b*, a gate insulating film **3** such as a nitride film or an oxide film is formed on the entire surface of the substrate in order to electrically insulate gate **2**. Semiconductor active layer **4** is then formed on insulating gate **2**. Active layer **4** is preferably made of amorphous silicon layer deposited by a chemical vapor deposition (CVD) process. Then, in order to reduce the contact resistance between the active layer and the subsequently formed source and drain, an impurity-doped semiconductor layer **5** is formed on amorphous silicon layer **4**, as an ohmic contact layer. Impurity-doped semiconductor layer **5** and amorphous silicon layer **4** are etched according to a predetermined active layer pattern.

As shown in FIG. **2***c*, a conductive layer for forming source electrode **7** and drain electrode **8** is deposited on the substrate by patterning a sputtered layer of conductive material. Using the source and drain electrodes as masks, portions of the impurity-doped semiconductor layer **5** are exposed and then etched. Source electrode **7** thus forms part of a transistor region and serves as source pad **7**A above the gate insulating film so that the same conductive layer constitutes part of the source wiring and the source electrode of the TFT.

As shown in FIG. **2***d*, a passivation layer **9**, e.g., a nitride film, is deposited on the entire surface of the substrate by a CVD process. Then, a predetermined portion of passivation layer **9** and gate insulating film **3** are selectively etched to form first, second and third contact holes **20**, **30** and **40**, thereby exposing a predetermined region of source pad **7**A above gate insulating film **3**, a predetermined region of drain electrode **8**, and a predetermined region of gate pad **2**C. For external electrical connections It is necessary to exposed pads **7**A and **2**C.

As shown in FIG. **2***e*, an indium tin oxide (ITO) layer is next deposited on the substrate by sputtering or a CVD process and etched according to a predetermined pattern to form a pixel electrode **6**. As further shown in FIG. **2***e*, pixel electrode **6** is connected to the upper portion of drain electrode **8** At the same time, ITO pattern **6**B is formed on gate pad **2**C. In addition, ITO pattern **6**A is provided on source pad **2**A, which is part of a data electrode of the LCD. The TFT of the present invention having electrical contacts or wiring structures including gate pad **2**C, layer **6**B and layer **6**A, source pad **7**A is thus completed.

As described above, the pixel electrode **6** is formed after the passivation process in the present invention. In contrast, pixel electrode **6** is formed after the pad process or the source/drain formation process in the conventional method. Thus, the passivation layer is interposed between the source/drain formation material and the pixel electrode, thereby effectively isolating these layers and preventing shorts.

Further, unlike the conventional process, the method in accordance with the present invention does not require the step of exposing the pad directly after depositing the gate insulating film, and the source and gate pads are exposed by etching during the passivation process. Thus, the pixel electrode, which is made of ITO, is formed on the source and gate pads. In addition, the source pad is not formed of gate material, but is formed from the source formation material, while the source and drain are deposited. Thus, the problem of high contact resistance between the source pad and the source, caused by forming the source pad from the gate material, can be avoided.

FIG. **3** illustrates a second embodiment of the present invention in which the step of etching the gate insulating layer and the step of etching the passivation layer to expose the pads are preformed in only one mask step. In particular, source pad **2**A is composed of gate material, as in the conventional method, and is formed at the same time as gate **2**, storage capacitor electrode **2**D and gate pad **2**B. After forming first, second, third and fourth contact holes **45**, **50**, **55** and **60**, material for forming the pixel electrode is then deposited. As a result, since both the first (**45**) and fourth (**60**) contact holes are formed over source pad **2**A (formed of the same material as the gate) and source electrode **7**, respectively, the source electrode **7** and source pad **2**A may be connected to each other in the same step that the pixel electrode is formed. Thus, after patterning, a first transparent conductive layer **6**C connects source electrode **7** with source pad **2**A, and a second transparent conductive layer **6** (i.e., the pixel electrode) is connected to drain electrode **8**.

In other words, a conductive layer is formed on a transparent glass substrate **1** and patterned to form gate **2**, a storage capacitor electrode **2**D,. a source pad **2**A and a gate

pad 2B. After forming a gate insulating film 3 on the entire surface of the substrate, an amorphous silicon layer 4 and an impurity-doped semiconductor layer 5 are sequentially formed therson. These layers are then etched in accordance with a predetermined active layer pattern.

Then, a conductive layer is formed on the substrate and etched in accordance with a predetermined pattern, thereby forming a source electrode 7 and a drain electrode 8. After forming a passivation layer 9 on the entire surface of the substrate, passivation layer 9 and gate insulating film 3 are selectively etched, thereby forming a first contact hole exposing the source pad 2A and a third contact hole exposing the gate pad 2B. Since the passivation layer 9 and gate insulating film 3 are preferably etched in a single step, the sidewalls of the first and second contact holes are planar and smooth.

ITO is then deposited on the entire surface of the substrate and patterned to form a pixel electrode 6 connected to drain electrode 8 through the contact hole overlying drain electrode 8 in the pixel part. At the same time, ITO patterns 6A, 6B and 6C are formed to contact source pad 2A and gate pad 2B through the contact holes formed at gate insulating film 3 and passivation layer 9.

Further, in accordance with an additional embodiment of the present invention, a repair line or static electricity protection circuit can also be provided during deposition of the pixel electrode layer. FIG.4 is a schematic diagram of static electricity protection circuit 100, and FIG.5 is an enlarged cross-sectional view of a portion 150,of the circuit.

In the circuit shown in FIG.4. if a high potential due to an electrostatic discharge is present on source electrode 7, for example, transistor 170 is rendered conductive to discharge source electrode 7 to gate line 2. Similarly, gate line 2 can discharge to source electrode 7 via transistor 160. As shown in FIG.5, the connection between gate line 2 and source electrode 7 is achieved by forming contact holes in insulative films 3 and 9 and then depositing conductive material (preferabel ITO) into these holes while forming the pixel electrode.

According to the present invention as described above, the manufacture of the TFT of the liquid crystal display device can be accomplished using five mask steps (step of forming the gate, step of forming the active layer, step of forming the source and drain, step of etching the passivation layer and gate insulating film, and step of forming the pixel electrode), while the conventional process requires six or more mask steps. Thus, manufacturing cost can be reduced.

Further, when the source pad is formed from the same material as the source electrode, the contact resistance problem caused when the source pad is in contact with the source electrode can be solved. In addition, since the pixel electrode is formed after forming the passivation layer, processing errors resulting in the pixel electrode contacting the source and drain can be prevented.

Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention disclosed herein. It is intended that the specification and examples be considered as exemplary only, with a true scope and spirit of the invention being indicated by the following claims.

What is claimed is:

1. A wiring structure comprising:

a substrate;

a first conductive layer formed on a first portion of said substrate;

a first insulative layer formed on a second portion of said substrate and on said first conductive layer;

a second conductive layer formed on a first portion of said first insulative layer;

a second insulative layer formed on said second conductive layer and on a second portion of said first insulative layer overlying said first conductive layer;

an indium tin oxide layer formed on said second insulative layer,

wherein a first contact hole is provided through said first and second insulative layers to expose part of said first conductive layer and a second contact hole is provided through said second insulative layer to expose part of said second conductive layer, said indium tin oxide layer extends through said first and second contact holes to electrically connect said first conductive layer with said second conductive layer, and

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

2. A wiring structure comprising:

a substrate;

a first conductive layer formed on a portion of said substrate;

a first insulative layer having a first via hole exposing a portion of said first conductive layer;

a second conductive layer formed on a portion of said first insulative layer;

a second insulative layer having a second via hole exposing said exposed portion of the first conductive layer and having a third via hole exposing a portion of the second conductive layer;

a third conductive layer formed on said second insulative layer and electrically connecting said first conductive layer to said second conductive layer through said first, second, and third via holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

3. A wiring structure in accordance with claim 2, wherein said third conductive layer includes indium tin oxide.

4. A wiring structure in accordance with claim 2, wherein said first and second via holes constitute a common hole exposing said exposed portion of said first conductive layer, a sidewall of said common hole being substantially smooth.

5. A wiring structure in accordance with claim 2, wherein said second via hole is aligned with said first via hole.

6. A liquid crystal display device comprising:

a substrate having a primary surface;

a first conductive layer disposed on a predetermined region of said primary surface;

a first insulating layer formed overlying said primary surface including said first conductive layer, said first insulating layer including a first contact hole exposing a predetermined portion of said first conductive layer;

a second conductive layer formed on a predetermined region of said first insulating layer;

a second insulating layer formed overlying said primary surface including said second conductive layer, said second insulating layer having a second contact hole exposing a predetermined portion of said second conductive layer and said first contact hole region; and

a third conductive layer formed on said second insulating layer and electrically connected to said first and second conductive layers via said first and second contact holes,

wherein one of said first and second conductive layers is connected to one of a plurality of terminals of a thin film transistor.

7. A liquid crystal display device in accordance with claim **6**, wherein said third conductive layer includes material suitable for forming a pixel electrode.

8. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer pattern on a substrate, said first conductive layer pattern being connected to a first terminal of a thin film transistor;

forming a first insulating layer overlying a surface of said substrate including said first conductive layer pattern;

forming a second conductive layer pattern on said first insulating layer, said second conductive layer pattern being connected to a second terminal of the thin film transistor;

forming a second insulating layer overlying said substrate including said second conductive layer pattern;

selectively etching said first and second insulating layers to form a first contact hole and a second contact hole exposing said first conductive layer pattern and said second conductive layer pattern, respectively; and

forming a third conductive layer on said second insulating layer, said third conductive layer electrically connected to said first and second conductive layer patterns via said first and second contact holes, respectively.

9. A method of manufacturing a liquid crystal display device in accordance with claim **8**, wherein said selective etching step is performed in a single etch step and said third conductive layer includes indium tin oxide.

10. A liquid crystal display device comprising:

a substrate;

a first conductive layer on said substrate including:
a gate electrode,
a gate pad, and
a source pad;

a gate insulating film on said surface of said substrate,

a portion of said gate insulating film overlying said gate electrode;

a semiconductor layer on said portion of said gate insulating film;

an impurity-doped semiconductor layer on said semiconductor layer;

a source electrode and a drain electrode on said semiconductor layer;

a passivation layer overlying said source pad, said drain electrode, said gate pad, and said source electrode;

a first contact hole provided through said passivation layer and said gate insulating film exposing said source pad;

a second contact hole provided through said passivation layer exposing said drain electrode;

a third contact hole provided through said passivation layer and said gate insulating film exposing said gate pad;

a fourth contact hole provided through said passivation layer exposing said source electrode;

a pixel electrode electrically connected with said drain electrode via said second contact hole; and

a transparent conductive layer electrically connecting said source pad with said source electrode via said first contact hole and said fourth contact hole.

11. A method of manufacturing a liquid crystal display device, comprising the steps of:

forming a first conductive layer on a substrate;

patterning said first conductive layer to form a gate electrode, a gate pad and a source pad;

forming an insulating film on said substrate including said patterned conductive layer;

forming a semiconductor layer on said insulating film;

forming an impurity-doped semiconductor layer on said semiconductor layer;

patterning said impurity-doped semiconductor layer and said semiconductor layer to form an active layer;

forming a second conductive layer overlying said substrate including said active layer;

patterning said second conductive layer to form source electrode and a drain electrode on said active layer;

forming a passivation film overlying said substrate including said source pad, a portion of said drain electrode, said gate pad portion, and a portion of said source electrode;

selectively etching said passivation film and said insulating film to form a first contact hole exposing said source pad, a second contact hole exposing said portion of said drain electrode, a third contact hole exposing said gate pad portion, and a fourth contact hole exposing said portion of said source electrode;

patterning a pixel electrode electrically connected to said drain electrode via said second contact hole;

patterning a first transparent conductive layer electrically connected to said gate pad through said third contact hole; and

patterning second transparent conductive layer electrically connecting said source pad to said source electrode via said first and fourth contact holes.

* * * * *

EXHIBIT C

United States Patent [19]

Shimbo

[11] **Patent Number: 4,624,737**

[45] **Date of Patent: Nov. 25, 1986**

[54] **PROCESS FOR PRODUCING THIN-FILM TRANSISTOR**

[75] Inventor: **Masafumi Shimbo, Tokyo, Japan**

[73] Assignee: **Seiko Instruments & Electronics Ltd., Tokyo, Japan**

[21] Appl. No.: **743,092**

[22] Filed: **Jun. 10, 1985**

[30] **Foreign Application Priority Data**

Aug. 21, 1984 [JP] Japan 59-173848

[51] **Int. Cl.**[4] **H01L 21/306; B44C 1/22; C03C 15/00; C23F 1/02**

[52] **U.S. Cl.** ..... **156/643;** 29/576 R; 29/578; 29/591; 156/652; 156/653; 156/656; 156/657; 156/659.1; 156/662; 156/667; 357/4; 357/23.1; 427/88; 427/93; 427/94

[58] **Field of Search** ..... 156/643, 646, 652, 653, 156/655, 656, 657, 659.1, 661.1, 662, 667, 668; 204/192 E, 192 EC; 427/38, 39, 88, 89, 90, 93, 94, 95; 430/313, 317, 318; 29/571, 576 R, 578, 591; 357/4, 23.1, 23.7, 65, 71

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Primary Examiner—William A. Powell
Attorney, Agent, or Firm—Robert E. Burns; Emmanuel J. Lobato; Bruce L. Adams

[57] **ABSTRACT**

A gate insulating film, a high-resistivity semiconductor film, a low-resistivity semiconductor film and if necessary a conducting film are successively deposited in lamination without exposing them to any oxidizing atmosphere including atmospheric air, and then the source and drain electrodes are selectively formed.

4 Claims, 13 Drawing Figures

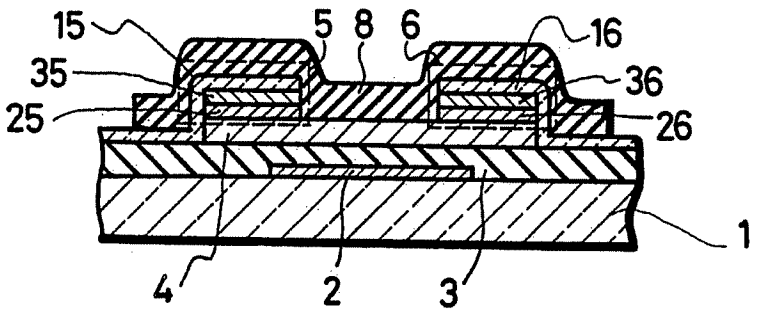


FIG. 1a PRIOR ART

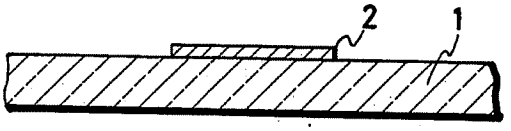


FIG. 1b PRIOR ART

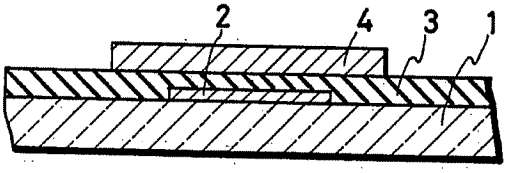


FIG. 1c PRIOR ART

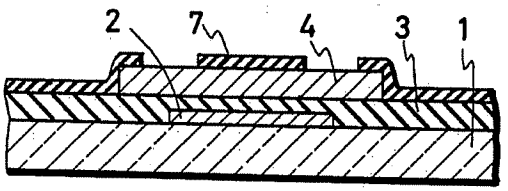


FIG. 1d PRIOR ART

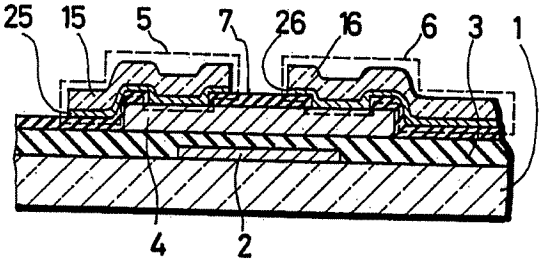


FIG. 2a

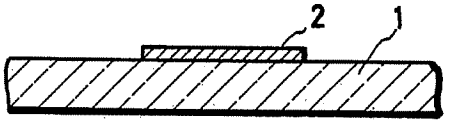


FIG. 2b

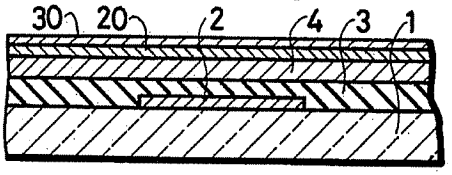


FIG. 2c

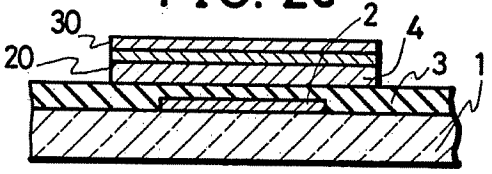


FIG. 2d

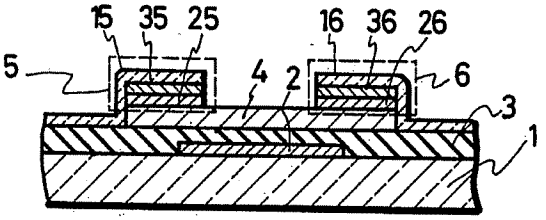


FIG. 2e

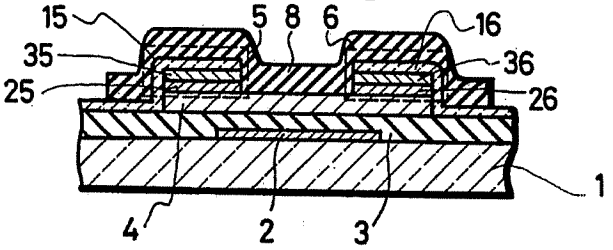


FIG. 3a

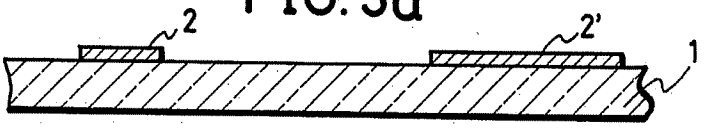


FIG. 3b

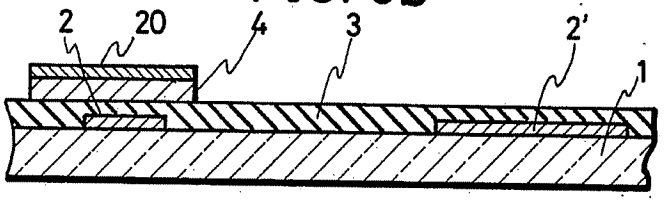


FIG. 3c

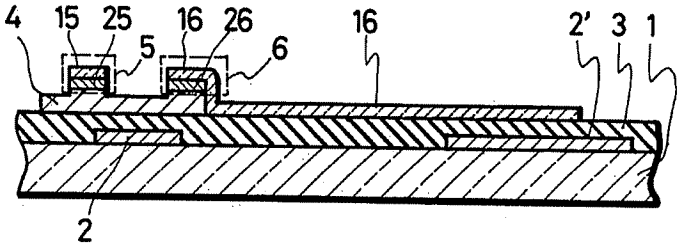
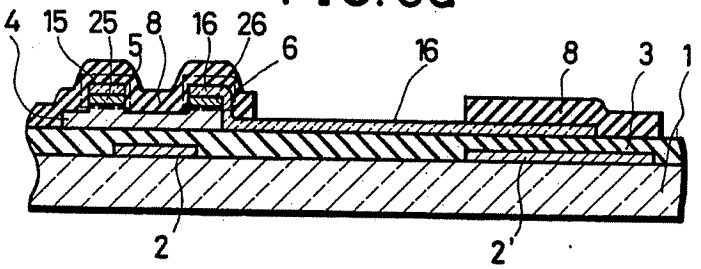


FIG. 3d



PROCESS FOR PRODUCING THIN-FILM TRANSISTOR

BACKGROUND OF THE INVENTION

This invention relates to a process for producing a thin-film transistor with improved performance.

Thin-film transistors (TFT) using semiconductor films of amorphous silicon (a-Si) or polycrystalline silicon (P-Si) are being applied to liquid crystal displays and like devices. Such thin-film transistors are diversified in structure. FIGS. **1***a* to **1***d* illustrate a conventional process for producing a thin-film transistor of a planar structure using amorphous silicon film. Shown in FIG. **1***a* in a sectional view is the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as a glass substrate. Then, as shown in FIG. **1***b*, a gate insulating film **3** (such as silicon nitride film) and an amorphous silicon film **4** are continuously deposited, and said amorphous silicon film **4** is selectively etched. Then a field insulating film **7** (such as SiOx film) is deposited and windows for contact with source and drain regions are formed as shown in FIG. **1***c*. Although not shown, a gate contact window is also formed simultaneously. Thereafter, as illustrated in FIG. **1***d*, for instance n^+ amorphous silicon films **25**, **26** and metal (such as Al) films **15**, **16** are deposited and selectively etched to form drain and source electrodes **5**, **6**, thereby completing a thin-film transistor unit. If necessary, a surface passivation film and/or light-shielding film are further formed thereon.

In the conventional process shown in FIGS. **1***a* to **1***d*, since the masking step precedes the deposition of n^+ amorphous films **25**, **26**, natural oxide is produced on the exposed surface of amorphous silicon film **4**. Although such natural oxide can be removed by an aqueous solution of hydrofluoric acid (HF) or a similar substance, the possibility is still great that oxygen and its compounds as well as other impurities can collect on the laminate surface as it is exposed to the atmosphere. This would give rise to electrical resistance between the source and drain and between channels in the thin-film transistor thus obtained, making such transistor unable to exhibit its desired characteristics. A similar phenomenon would also occur at the interface of n^+ amorphous silicon films **25**, **26** and metal films **15**, **16**.

As described above, according to the conventional process, resistance would be generated between the source and drain and between channels and it was thus impossible to obtain the proper current flow and frequency characteristics. It was also a disadvantage of such conventional process that it was necessary to repeat the masking step as many as 5 to 6 times.

SUMMARY OF THE INVENTION

It is an object of present invention to provide a simplified process for producing a thin-film transistor with an improved contact arrangement.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. **1***a* to **1***d* are sectional views showing the sequential steps in a conventional thin-film transistor production process.

FIGS. **2***a* to **2***e* are sectional views illustrating stepwise a process for producing a thin-film transistor according to the present invention.

FIGS. **3***a* to **3***d* are sectional views illustrating the sequential steps for producing a thin-film transistor according to the process of this invention as it was applied to a substrate for liquid crystal display.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The present invention will be described in detail below with reference to the accompanying drawings.

FIGS. **2***a* to **2***e* are sectional views illustrating a process for producing a thin-film transistor using amorphous silicon according to this invention. FIG. **2***a* shows in a sectional view the initial step for selectively forming a gate electrode **2** on an insulating substrate **1** such as glass, quartz, ceramic, insulator-coated silicon or metal. Metals such as Cr, Mo, W, Al, Ta, etc., and their silicides, impurity-doped polysilicon and other like materials can be used as said gate electrode **2**.

In the next step illustrated in FIG. **2***b* in a sectional view, a gate insulating film **3**, a high-resistivity film **4**, a low-resistivity a-Si:H (usually hydrogenated amorphous silicon) film **20** and a conducting film **30** made of a metal or other material are successively formed on said gate electrode **2** and substrate **1** without exposing them to an oxidizing atmosphere. Such successive deposition can be accomplished, for instance, by forming a silicon nitride (SiNx) film as gate insulating film **3** from a mixed gas of SiH_4 and NH_3, forming a high-resistivity a-Si:H film **4** by using SiH_4 and forming a n^+ a-Si:H film **20** from a mixed gas of PH_3 and SiH_4 in the same evacuated chamber in a plasma CVD apparatus. It is also possible to form said films successively in the respective chambers by using a plasma CVD apparatus having in-line chambers. Further, when a sputtering or metalizing chamber is additionally provided, conducting film **30** can be also deposited continuously without exposure to the atmosphere. Beside SiNx, a film of SiOx or a multi-layer film made of such materials can be used as said gate insulating film **3**. In place of said high-resistivity amorphous silicon film **4**, there can be used a film of amorphous silicon-fluorine alloy (a-Si:F) or amorphous silicon-hydrogen-fluorine alloy (a-Si:H:F) using, for instance, SiF_4, or a microcrystalline amorphous silicon film. Such alloys can be also used for said low-resistivity amorphous silicon film **20**, and such film may contain other impurites beside phosphorous impurities. As said conducting film **30**, it is desirable to use a stable conducting film such as a transparent conducting film made of a refractory metal such as Cr, W, Mo, Ta, etc., and silicides thereof, or indium-tin-oxide (ITO), SnO_2 and the like. Use of a transparent conducting film has the advantage that the process is simplified when the thin-film transistor of this invention is applied to an active matrix liquid crystal display.

FIG. **2***c* illustrates the step in which said conducting film **30**, low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region by etching in a single masking step. Known etching techniques such as wet etching, plasma etching, reactive ion etching, ion etching, etc., can be used for this step. Then, as illustrated in FIG. **2***d* in a sectional view, drain and source electrode members **15**, **16** are selectively provided, and conducting film **30** and low-resistivity amorphous silicon film **20** shown in FIG. **2***c* are selectively removed with said electrode members **15**, **16** serving at least as a part of the mask to form drain electrode **5** and source electrode **6**. In this step, it is desirable to clean the surface of conducting film **30** by proper etching means such as sputter etching or ion

etching before forming said drain and source electrode members **15, 16**. In this case, the channel areas of the thin-film transistor are safe from damage by cleaning as they are covered with conducting film **30**. The same materials as used for conducting film **30** and other materials such as Al can be used for said drain and source electrode members **15, 16**. When selectively etching low-resistivity amorphous silicon film **20**, no problem arises even if it is overetched to the extent that etching reaches the high-resistivity amorphous silicon film **4**.

In the final step illustrated in FIG. 2*e*, a surface passivation film **8** is deposited, and the drain and source electrodes **15, 16** and gate electrode **2** are partly exposed (not shown). A CVD film of SiOx, SiNx, etc., a resist or a coating of polyimide resin can be used as said surface passivation film **8**. If light shielding is required, a multilayer film composed of said insulating film and a metal or high-resistivity semiconductor film can be used as said surface passivation film **8**. When amorphous silicon-germanium alloy ($a\text{-}Si_{1-x}Ge_x$) is used as light-shielding film, surface passivation may not be necessary.

FIGS. 3*a* to 3*d* show sectionally a unit picture cell in an application of the present invention to the manufacture of a TFT substrate for liquid crystal display. FIG. 3*a* illustrates a step in which gate electrode **2** extending along one line and gate electrodes **2'** on another line are formed on a transparent insulating substrate **1** such as glass substrate. Then, as illustrated in FIG. 3*b*, gate insulating film **3**, high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20** are deposited successively without exposure to an oxidizing atmosphere, and said low-resistivity amorphous silicon film **20** and high-resistivity amorphous silicon film **4** are left as an island region in the area where a thin-film transistor is to be formed.

In the next step illustrated in FIG. 3*c*, a transparent conducting film such as ITO film is deposited; then, drain electrode **15** and source electrode **16** which doubles as a picture cell electrode are selectively formed and the exposed portion of low-resistivity amorphous silicon film **20** is removed. In this example, a charge-holding capacitor is formed by said picture cell electrode (source electrode) **16**, gate electrode **2'** and gate insulating film **3**. In the final step shown sectionally in FIG. 3*d*, surface passivation film **8** concurrently serving as a light-shielding film is deposited and then selectively etched to expose picture cell electrode, drain electrode **15** and a part of gate electrodes **2, 2'** (not shown). In this example, no conducting film is formed on low-resistivity amorphous silicon film **20**, but a conducting film such as ITO film may be formed on said low-resistivity film **20** as in the example shown in FIG. **2**.

As described above, according to the present invention, no oxides, etc., are formed at the interface of high-resistivity amorphous silicon film **4** and low-resistivity amorphous silicon film **20**, so that a good junction can be formed. The same is true with the interface of low-resistivity amorphous silicon film **20** and conducting film **30**. Further, since the interfaces of low-resistivity amorphous silicon film **20** or conducting film **30** and drain and source electrodes **15, 16** can be cleaned without damaging the high-resistivity amorphous silicon film, a good contact can be obtained without sacrificing the inherent properties of thin-film transistor.

According to the present invention, as explained above, a thin-film transistor having good contact characteristics can be formed with only four masking operations. The present invention is especially effective for the production of thin-film transistors requiring a low temperature process such as thin-film transistors using amorphous silicon. It is thus possible with the present invention to obtain a thin-film transistor with small channel series resistance which improves driving performance and frequency characteristics.

While the present invention has been principally described regarding an embodiment thereof as applied to the production of a thin-film transistor using amorphous silicon by utilizing plasma CVD, the invention can as well be applied to the manufacture of thin-film transistors using semiconductor films by utilizing the photo CVD or molecular beam and/or the ion beam deposition method, thin-film transistors using polysilicon, and thin-film transistors using semiconductor films of other materials than silicon; consequently, the present invention is of great industrial significance.

I claim:

1. A process for producing a thin-film transistor comprising a first step for forming a gate electrode on an insulating substrate, a second step for continuously depositing on said gate electrode and substrate a gate insulating film, a high-resistivity semiconductor film and a conducting film containing at least a low-resistivity semiconductor film without exposing them to an oxidizing atmosphere, a third step in which said high-resistivity semiconductor film and said conducting film are selectively etched so that they are partly left as an island region on said gate electrode, a fourth step for selectively forming a source electrode and a drain electrode both contacting a part of the surface of said island region and spaced apart from each other, a fifth step for selectively removing said conducting film exposed on said island region with said source and drain electrodes serving as at least a part of the mask, a sixth step for depositing a surface passivation film, and a seventh step for selectively removing said surface passivation film and exposing a part of each of said source electrode, drain electrode and gate electrode.

2. A process for producing a thin-film transistor according to claim **1**, wherein in said second step said conducting film is composed of at least two layers consisting of a low-resistivity semiconductor film and thereon a refractory metal film or transparent conducting film, and both of said films are continuously deposited without being exposed to the oxidizing atmosphere.

3. A process for producing a thin-film transistor according to claim **1** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

4. A process for producing a thin-film transistor according to claim **2** , wherein in said sixth step a light-shielding film is formed at a part of said surface passivation film.

* * * * *

EXHIBIT D

US006008786A

United States Patent [19]

Kimura et al.

[11] Patent Number: 6,008,786

[45] Date of Patent: Dec. 28, 1999

[54] **METHOD FOR DRIVING HALFTONE DISPLAY FOR A LIQUID CRYSTAL DISPLAY**

[75] Inventors: **Yasuhiro Kimura**, Yamato; **Haruhiro Matino**, Kanagawa-ken, both of Japan

[73] Assignee: **International Business Machines Corporation**, Armonk, N.Y.

[21] Appl. No.: **08/832,640**

[22] Filed: **Apr. 4, 1997**

[30] **Foreign Application Priority Data**

May 22, 1996 [JP] Japan 8-127173

[51] **Int. Cl.**[6] **G09G 3/36**

[52] **U.S. Cl.** **345/89**; 345/153

[58] **Field of Search** 348/181, 500; 345/150, 22, 88, 153, 155, 89; 349/74

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Primary Examiner—Richard A. Hjerpe
Assistant Examiner—Ronald Laneau
Attorney, Agent, or Firm—Jay P. Sbrollini

[57] **ABSTRACT**

To correct the dependency of the transmissivity/applied voltage characteristics on color, a computing circuit is provided for generating corrected gray scale data by performing an addition or subtraction of the gray scale level related to at least one color. A delay circuit delays the gray scale data for uncorrected colors to maintain synchronization between the gray scale signals of all colors.

13 Claims, 6 Drawing Sheets

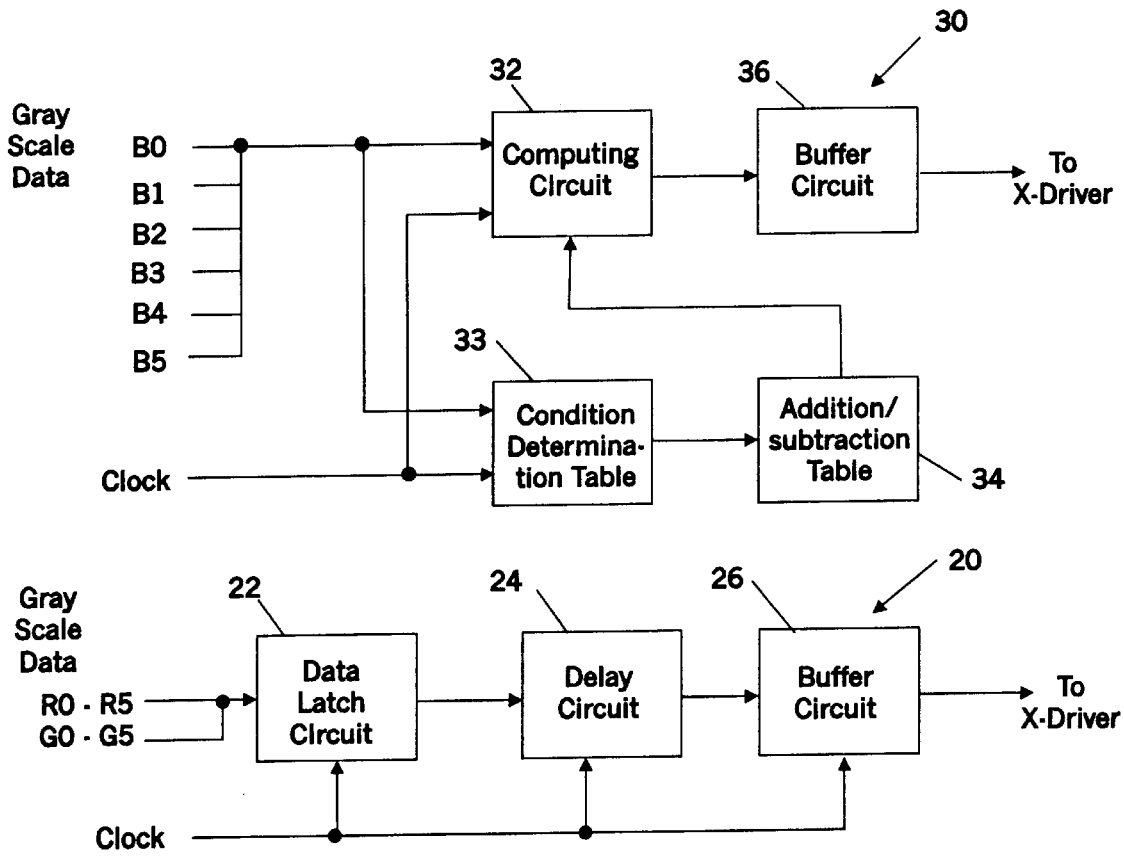


FIG. 1

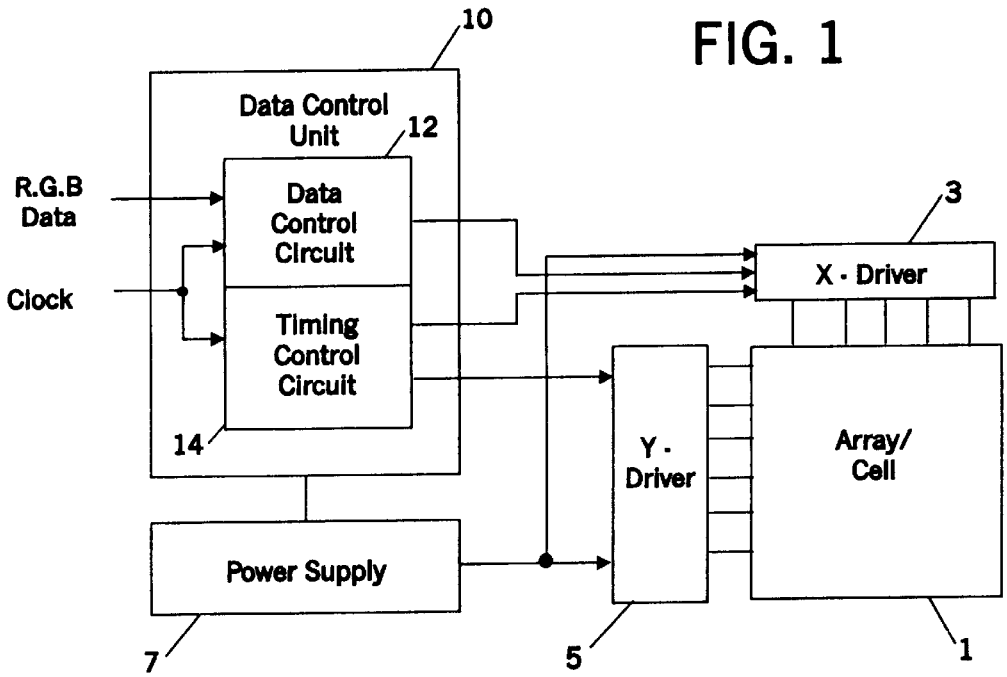
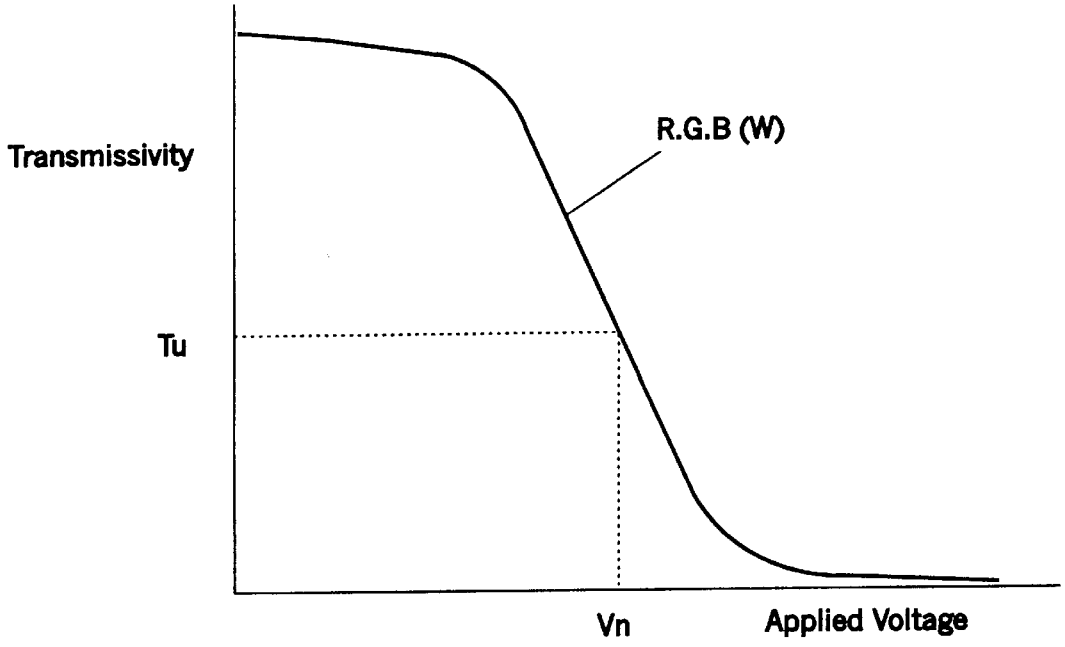

10
Data Control Unit
12
R.G.B Data
Clock
Data Control Circuit
Timing Control Circuit
14
3
X - Driver
Y - Driver
Array/ Cell
Power Supply
7
5
1

FIG. 2


Transmissivity
R.G.B (W)
Tu
Vn
Applied Voltage

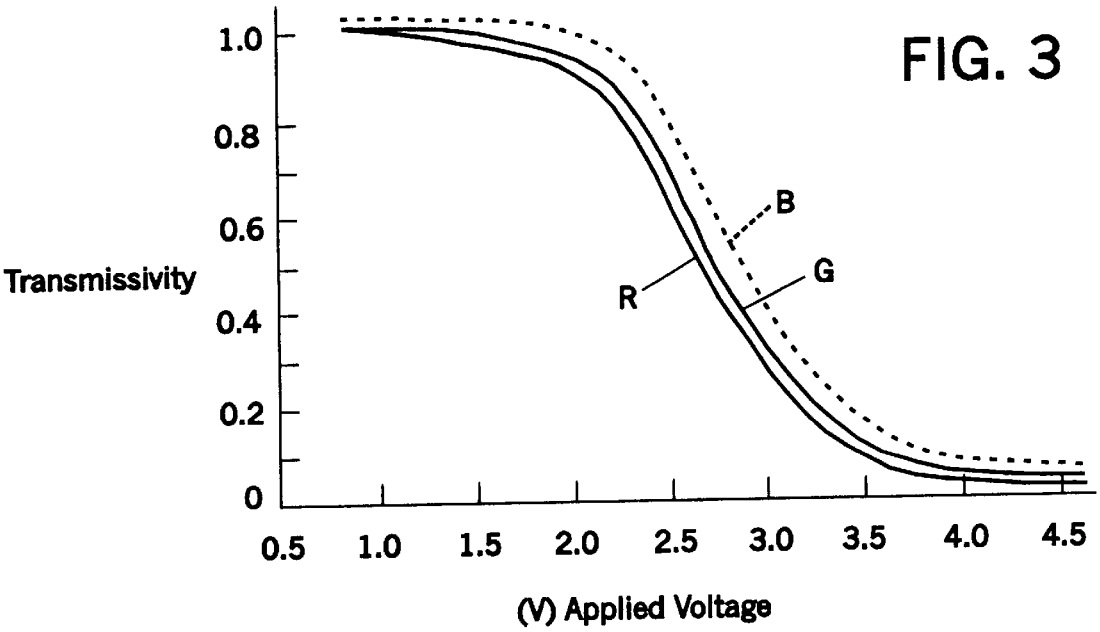

1.0
0.8
0.6
0.4
0.2
0
Transmissivity
B
G
R
0.5
1.0
1.5
2.0
2.5
3.0
3.5
4.0
4.5
(V) Applied Voltage

FIG. 3

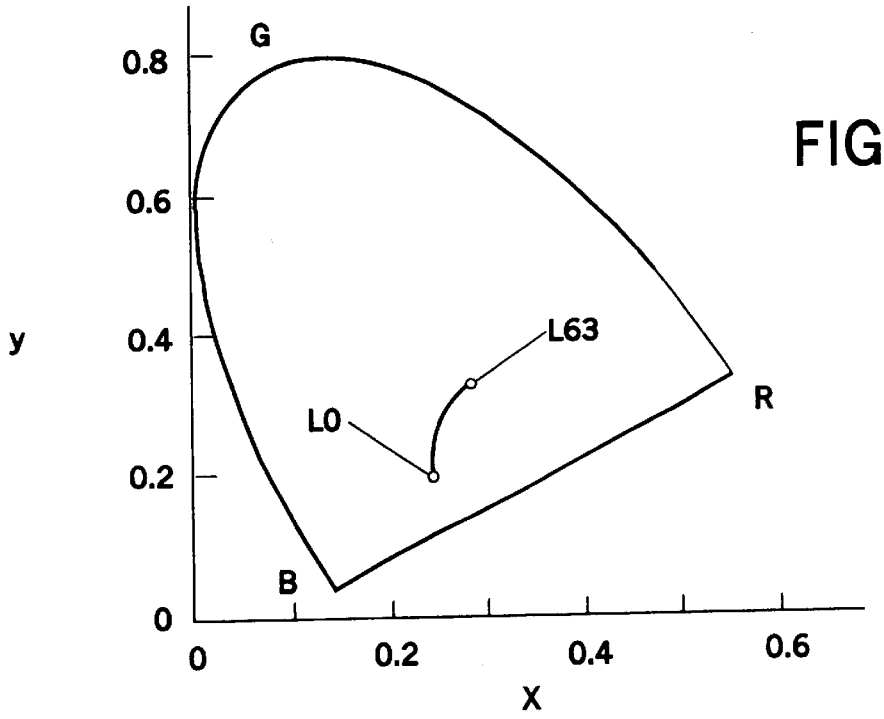
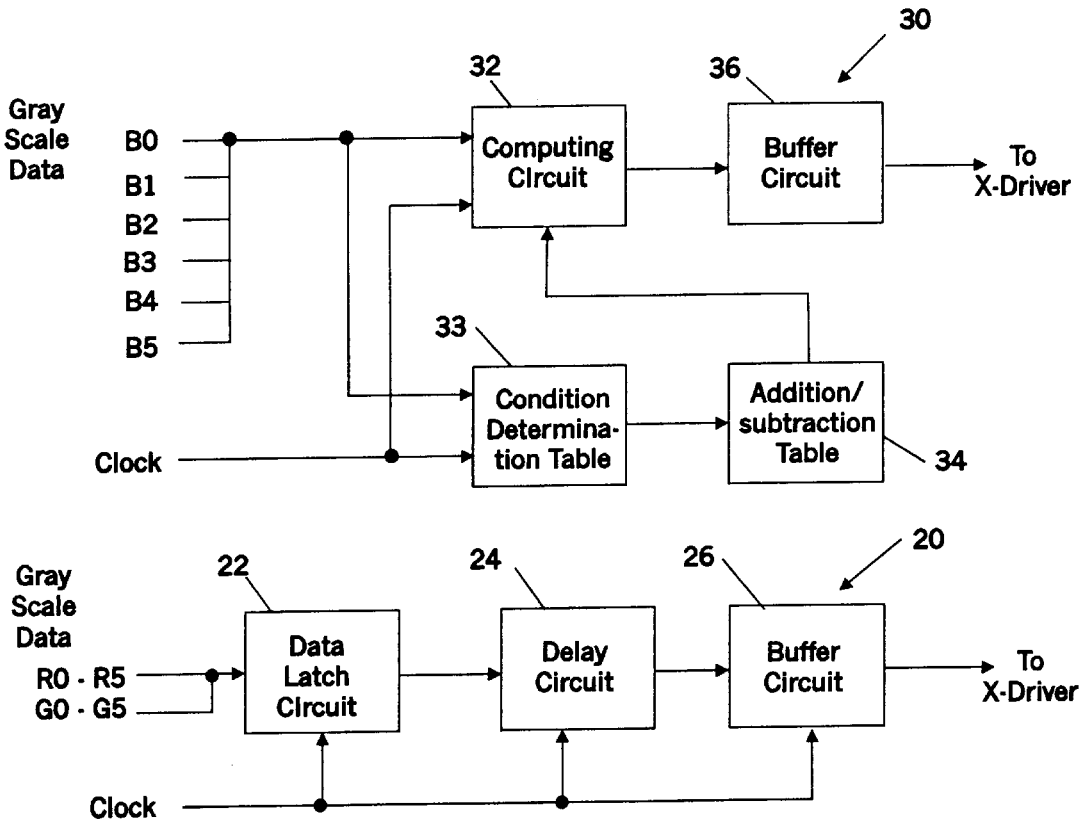

G
0.8
0.6
y
0.4
0.2
0
L63
L0
R
B
0
0.2
0.4
0.6
X

FIG. 4

FIG. 5


30
32
36
Gray Scale Data
B0
B1
B2
B3
B4
B5
Computing Circuit
Buffer Circuit
To X-Driver
33
Condition Determina-tion Table
Addition/ subtraction Table
34
Clock
20
22
24
26
Gray Scale Data
R0 - R5
G0 - G5
Data Latch Circuit
Delay Circuit
Buffer Circuit
To X-Driver
Clock

Gray Scale	Condition
0 - 3	A
4 - 10	B
11 - 53	C
54 - 60	B
61 - 63	A

FIG. 6

FIG. 7

Condition	Addition/ Subtraction Amount
A	0
B	−2
C	−4
⋮	⋮

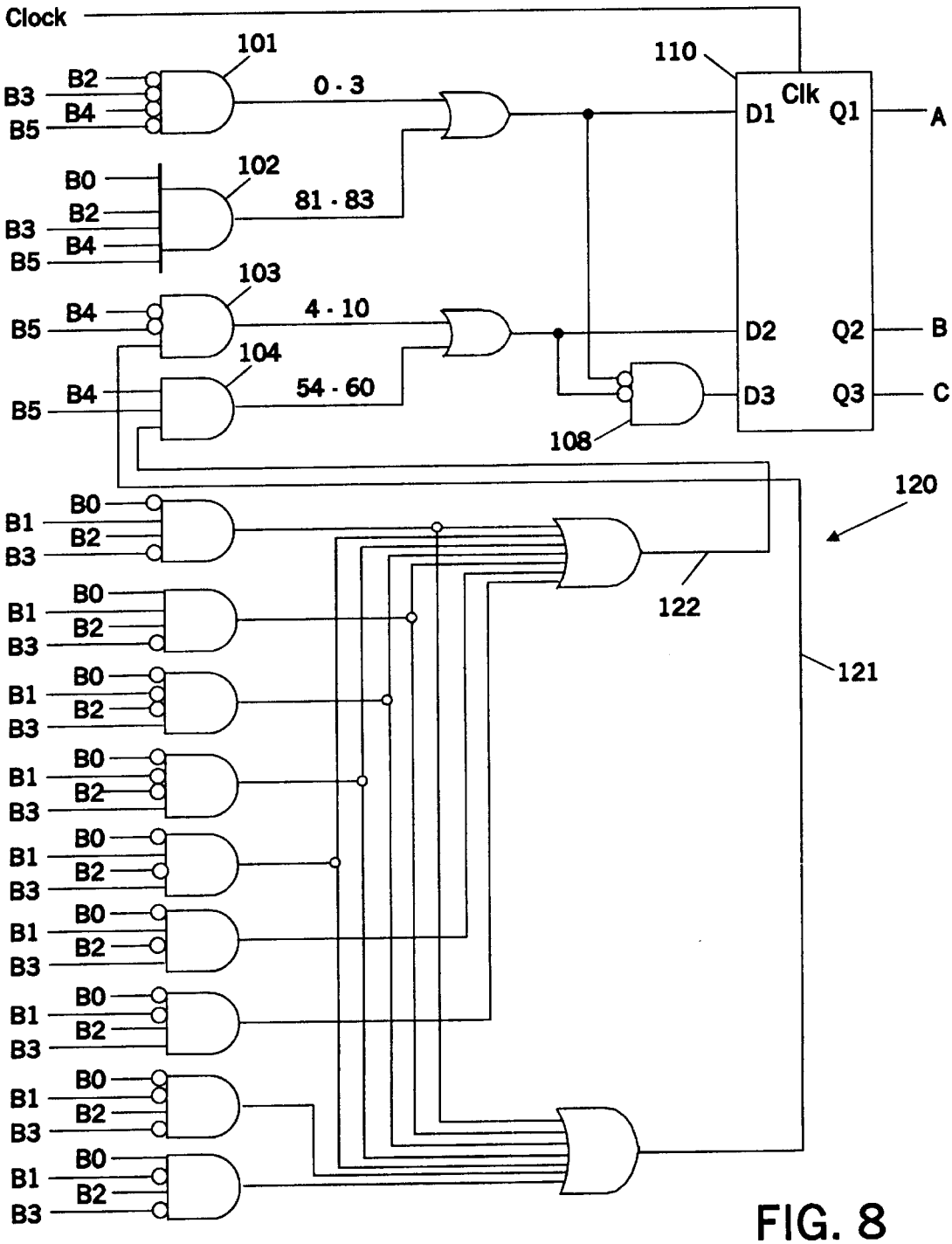
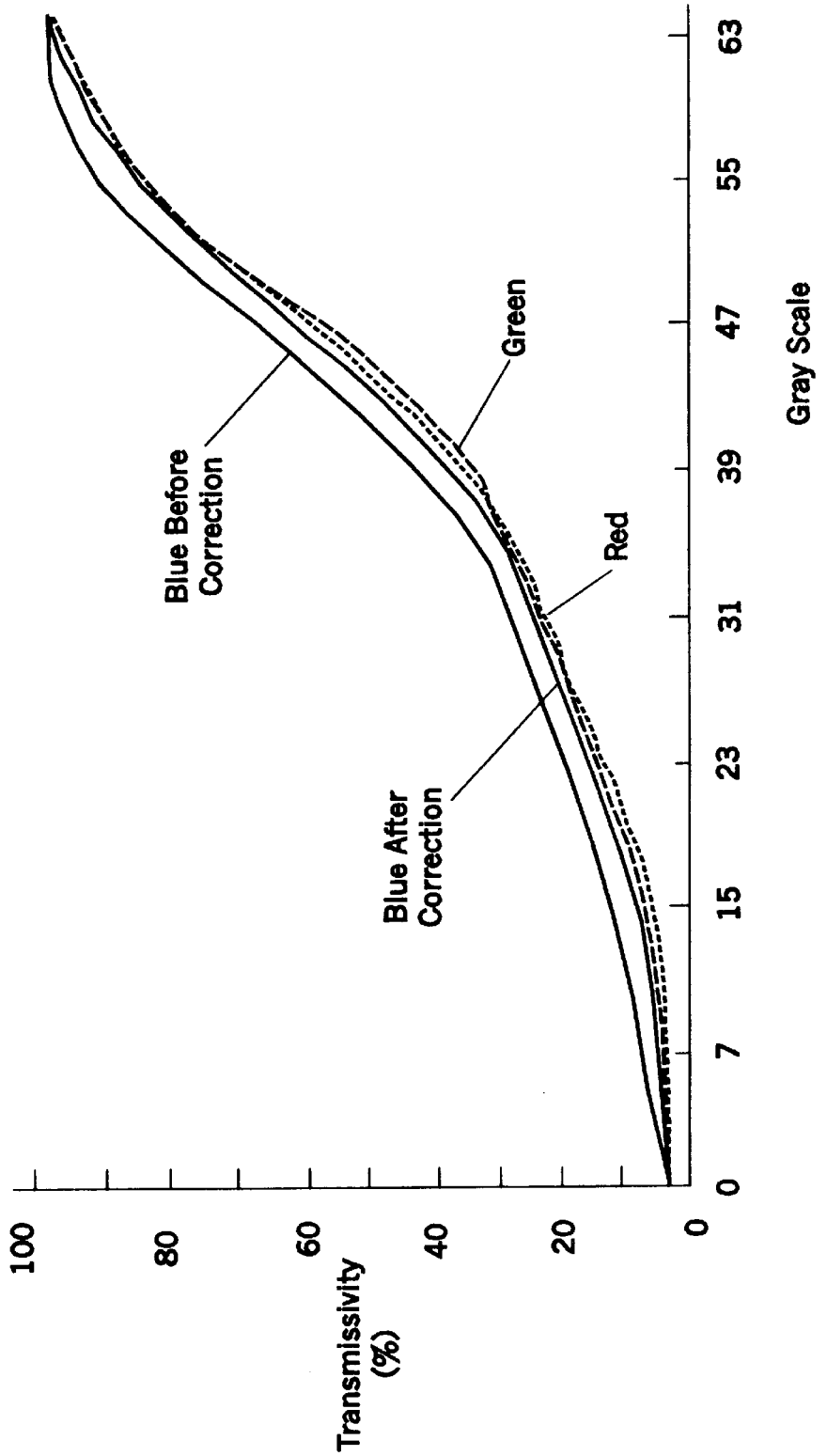

Clock
101
B2
B3
B4
B5
0 - 3
102
B0
B2
B3
B4
B5
81 - 83
103
B4
B5
4 - 10
104
B4
B5
54 - 60
110
Clk
D1
Q1
A
D2
Q2
B
D3
Q3
C
108
120
122
121
B0
B1
B2
B3

FIG. 8

FIG. 9


Blue Before Correction
Green
Red
Blue After Correction
Transmissivity (%)
100
80
60
40
20
0
0
7
15
23
31
39
47
55
63
Gray Scale

METHOD FOR DRIVING HALFTONE DISPLAY FOR A LIQUID CRYSTAL DISPLAY

FIELD OF THE INVENTION

The subject invention related to driving methods and control mechanisms in TFT liquid crystal displays (TFTLDCs). In particular, the subject invention relates to driving methods and control mechanisms for TFTLCD'S: in which the transition for each color in halftone display is effectively prevented.

BACKGROUND ART

The reduction in size of electronic equipment has been accompanied by an increase in the use of liquid crystal displays (LCDs). The LCD is not only used as a computer screen, but also is used as a television screen, a projection screen, etc. Utilizing liquid crystal has advantages such as low power consumption due to low driving voltage, and relatively fast response. It is expected that the field of application of LCDs will expand in the future.

Most of the currently used LCDs are of the active matrix type. The active matrix type means the one in which a separate driving circuit element is provided for each pixel to improve display characteristics. Active matrix LCDs using thin-film three-terminal transistors (TFTs) as switching elements are called TFT liquid crystal displays (TFTLCDs).

In using TFTLCDs to display pictures, it is necessary to provide gray scale data of the picture to the LCD to drive the LCD. FIG. **1** shows the construction of the control unit of the TFTLCD. The array/cell portion **1** of the LCD is connected to an X-driver **3** and a Y-driver **5**. The X-driver **3**, when it is supplied with gray scale data, applies a voltage corresponding to the gray scale data to the cell. The Y-driver **5** is connected to the gate of a switching element, and conducts/does not conduct the voltage applied to the cell by the X-driver **3** at a predetermined time.

Gray scale data is supplied to the X-driver by data control unit **10**. The data control unit **10** consists of a data control circuit **12** for latching and storing the externally supplied R/G/B data in a buffer, and a timing control circuit **14** for outputting the gray scale data stored in the buffer to the X-driver **3** at a predetermined time. A clock signal is externally supplied to the data control circuit **12** and the timing control circuit **14** to control the timing. A power supply **7** is connected to the X-driver, Y-driver **5**, and data control unit **10**.

To display a picture on an LCD, a voltage corresponding to the gray scale is provided to each pixel of each color. That is, the driving of a pixel is not a simple on-off function, a voltage divided into several levels (gray scales) is provided to adjust the transmissivity of the pixel, so that intermediate color intensity can be displayed. To achieve such control in a color display, R/G/B signal levels are supplied to each pixel. For a display of a 64-level gray scale, 64-step voltage is used, and the voltage for each pixel is applied according to the respective gray scale data. Ideally, the same transmissivity can be achieved for all the colors when the voltage corresponding to a particular gray scale is used. The relationship for this is shown in FIG. **2**. In FIG. **2**, transmissivity is plotted on the ordinate, and applied voltage is plotted on the abscissa. Applied voltage is determined by the gray scale data. Accordingly, when a certain gray scale n is chosen, the applied voltage Vn is determined by that gray scale. Then, according to the relationship of FIG. **2**, transmissivity Tn for the gray scale Vn is achieved.

Ideally, the relationship between gray scale, applied voltage, and transmissivity is the same for each of the R/G/B

colors. However in actuality, the gray scale and the achieved transmissivity have a slight difference depending on color. This is because the degree of light modulation for the specific twist of the twisted noematic liquid crystal is slightly different depending on wavelength. That is, even though a light passes through a liquid crystal layer in a similarly twisted state, the degree of the modulation given to the passing light is wavelength dependent, and thus the scattering of brightness that occurs for a given gray scale is color dependent. This is shown in FIG. **3**. The transmissivity of blue (B) is higher than that of both red (R) and green (G) for the same voltage over a wide range of applied voltage. That is, since the relationship between gray scale and applied voltage for each color is unique, the transmissivity of blue (B) is greater even if each color is selected with the same gray scale and the same voltage is applied in the displaying of intermediate colors. Thus, the correlation between transmissivity and applied voltage (hereinafter referred to as transmissivity/applied voltage characteristics) has a color (wavelength) dependency. If the displaying is performed without providing any correction, the graduation of color translates to blue more than called for by the halftone data, and the picture on the whole takes on a bluish hue. FIG. **4** shows this state represented by a chromaticity diagram. FIG. **4** shows that **L63** should be a white color state if an ideal state could be realized, but in actuality, **L0**, or a shift to blue, occurs because of the wavelength dependency of the transmissivity/applied voltage characteristics.

Various methods have been proposed for correcting the above problem. These methods are roughly divided into (1) methods for making the correction by the modification of the structure of LCD, and (2) methods for making the correction by using electric control.

A typical example of the first category (1) is the adoption of a multi-gap structure. A multi-gap structure is a structure in which the thickness of the color filter of the pixel of each color of R/G/B varies. That is, the thickness (gap) of the liquid crystal sealing portion is changed to achieve the matching of the transmissivity/applied voltage characteristics for each color. However, implementation of a multi-gap structure is accompanied by difficulties in the manufacturing process. Problems occur in the adjustment of the thickness of the color filter, and in the uniformization of the gap between the two glass substrates forming the liquid crystal cell. Yield is effected by these difficulties causing an increase in manufacturing cost.

As an example of the second category (2), is a method in which the reference voltage (gray scale voltage) given to the data driver is tailored to the characteristics for each color. This method can compensate for the color dependency of the transmissivity/applied voltage characteristics. However, the circuits needed to independently control the reference voltages, raise the cost and cause difficulties in the implementation. Another method that falls within this second category, is to use the voltage for one of the colors of R/G/B as a reference voltage, and use offset voltages for each of other colors. This methods has the same problems as the method in which the reference voltages are separately applied, and in addition, cannot accomplish desired effect if the gradients of the curves showing the transmissivity/applied voltage characteristics of R/G/B vary with applied voltage. That is, in accordance with the offset voltage method, correction is carried out by applying a uniform offset voltage for all applied voltages, and thus the correction cannot be effectively performed unless the gradients of the curves showing the transmissivity/applied voltage characteristics are the same over the whole applied voltage range.

Japanese Published Unexamined Patent Application No. 01-101586 discloses a technique in which different liquid crystal driving voltage levels are set for each of the colors, and that level is applied to each pixel. Japanese Published Unexamined Patent Application No. 03-6986 discloses a technique in which the driving voltage is made to vary a predetermined voltage from color to color to obtain uniformity in transmissivity. Japanese Published Unexamined Patent Application No. 03-290618 discloses a technique in which a similar object is accomplished by independently inputting a gray scale control signal for each color.

Therefore, first object of the subject invention is to provide a driving method for a TFTLCD in which the dependency on color of the transmissivity/applied voltage characteristics is effectively corrected.

A second object of the subject invention is to realize the effective correction using a very simple method which enables the above described correction to be made without increase in complexity of the control method, and the restrictions on the implementation by addition of circuits.

SUMMARY OF THE INVENTION

In accordance with the present invention, the above described problems are solved by gray scale data (a bit string for a color liquid crystal display) wherein the data control means includes a computing circuit for performing an addition or subtraction of the gray scale related to at least one color to generate a corrected gray scale, and also includes delay means for delaying the outputting of the uncorrected gray scales, during the time which the gray scale of the one color is being corrected.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a diagrammatic view of the driving circuit for TFTLCD according to the background art;

FIG. **2** is a graph showing the transmissivity/applied voltage characteristic in an ideal color LCD;

FIG. **3** is a graph showing the transmissivity/applied voltage characteristic of the color LCD in the background art;

FIG. **4** is a chromaticity diagram showing an example of the color transition of the color LCD in the background art;

FIG. **5** is a diagrammatic view of the data control unit in the driving circuit for TFTLCD according to the subject invention;

FIG. **6** is a diagrammatic view of the condition determination table in the data control unit according to the subject invention;

FIG. **7** is a diagrammatic view of the addition/subtraction table in the data control unit according to the subject invention;

FIG. **8** is a circuit for implementing by hardware the condition determination and the condition determination table in the data control unit according to the subject invention; and

FIG. **9** is a graph showing the transmissivity/applied voltage characteristic corrected by the driving circuit for TFTLCD according to the subject invention.

PREFERRED EMBODIMENT

The subject invention can be realized by improving the data control unit **10** of FIG. **1** as is shown in FIG. **5**. In the background art, the data control unit consists only of a latch and a buffer. However, in the subject invention, the gray scale data related to a color, that is to be corrected, is temporarily inputted to a computing circuit. An addition or subtraction operation is applied to that gray scale data to shift it by one or more gray scale levels, to thereby achieve transmissivity equivalent to the other colors which are not to be corrected.

In FIG. **5**, the color to be corrected is blue (B), and the colors which are not to be corrected are red (R) and green (G). The gray scale data related to R or G are shown by R**0** to R**5** or G**0** to G**5** in FIG. **5**.

A portion **20** to which gray scale data related to R and G are inputted includes a data latch circuit **22** and a buffer circuit **26**, like that in the data control unit in the background art. However, in addition to the data control unit in the background art, it includes a delay circuit **24**. This is to compensate for the time during which the gray scale data B**0** to B**5** related to B is operated on by a computing circuit **32** in accordance with a condition determination table **36**, as described later. The delay circuit **25** thereby assumes the outputting of the R and G gray scale data to the driver with the same timing as the corrected B gray scale data.

The gray data B**0** to B**5** for blue is a bit string for representing a 64-level gray scale. It is comprised of a bit string (B**0**, B**1**, B**2**, B**3**, B**4**, B**5**). For instance, if the gray scale is "4", (B**0**, B**1**, B**2**, B**3**, B**4**, B**5**)=(001000), and if the gray scale is "28", (B**0**, B**1**, B**2**, B**3**, B**4**, B**5**)=(001110). The same applied for R**0** to R**5** or G**0** to G**5** which are the gray scale data for reg or green, respectively.

Circuit **30** is for adjusting the Blue gray scale data B**0** to B**5**. To accomplish this, the gray scale data related to Blue is first supplied to a computing circuit **32**. In the computing circuit **32**, the gray scale data for blue is reduced, for instance, by zero to four levels in comparison with the grey scale data for red and green. By correcting gray scale data in this way, results in matching the transmissivity of blue to that of Red and Green.

Further, the gray scale data for Blue is also supplied to a condition determination table **33**. The condition determination table **33** determines the amount of the adjustment of the gray scale data. A diagrammatic representation of the condition determination table **33** is shown in FIG. **6**. As shown, conditions A to C, corresponding to various gray scale levels, are set in the condition determination table **33**. The condition corresponding to a gray scale is outputted from the condition determination table **33** to an addition/subtraction table **34**. The addition/subtraction table **34** has the function of setting the actual amount of the addition or subtraction. A diagrammatic representation of the addition/subtraction table **34** is shown in FIG. **7**. That is, the addition/subtraction tables set the amount to be added or subtracted according to the condition provided from the condition determination table **33**. The amount of the addition or subtraction to correct the gray scale is supplied to the computing circuit **32**.

The condition determination table **33** and the addition/subtraction table **34** can be implemented by software. The condition determination table can also be implemented by hardware by using the logic circuit shown in FIG. **8**. To implement the specific conditions represented in FIG. **6**, the gray scale data B**0** to B**5** are inputted to the logic circuit as shown. The gray scale data of B**2** to B**5** are inverted and inputted to an AND circuit **101** to create a condition corresponding to condition A in FIG. **6** for gray scale levels 0 to 3. Similarly, the gray scale data B**0**, B**2** to B**5** for gray scale levels 61 to 63 corresponding to condition A is inputted into AND circuit **102**. The outputs of the AND circuit **101** and the AND circuit **102** are inputted to an OR circuit **106**, and

the condition A is outputted by circuit **110**. AND circuit **103** and AND circuit **104** are circuits for generating condition B. Inputted to ANDs **103** and **104** is an output **122** separately created in a group of logic circuits **120**, to thereby output the condition B for desired gray scale data levels **4** to **10** and **54** to **60**. If there is no output from OR circuits **106** and **107**, condition C is set. In this case, an output is provided by an AND circuit **108** to the circuit **110** to achieve the generation of condition C. Conditions A, B, and C are outputted from Q1 to Q3 of the circuit **110**.

Operation of the circuit **30** to which gray scale data for blue is inputted, and of the circuit **20** to which gray scale data related to Red and Green are inputted is as follows. When a gray scale level "2" is received, or (B0, B1, B2, B3, B4, B5)=(010000) is inputted, the input to the display is determined by the condition determination table **33**. As shown in FIG. **6**, in the condition determination table **33**, the condition A is outputted to the addition/subtraction table **34**, and thereafter, in the addition/subtraction table **34**, "0" is outputted to the computing circuit as the addition or subtraction amount as shown in FIG. **7**. Accordingly, the gray scale "2" is provided unconnected to the X-driver via a buffer circuit **36**. The above described processing causes a predetermined delay. Thus, the gray scale data for Red and Green corresponding to the gray scale data related to Blue are delayed for time taken for the processing by a delay circuit **24**. As a result, the gray scale data related to B is outputted from the buffer circuit **36** to the X-driver is synchronized with the gray scale data for Red and Green for simultaneous output from the buffer circuit **26** to the X-driver.

Where the gray scale data level is "20," or the grey scale level signal (B0, B1, B2, B3, B4, B5)=(001010), the condition determination table **33** provides condition C signal to the addition/subtraction table **34** as shown in FIG. **6**. In response, the addition/subtraction table **34** provides a signal to the computing circuit to subtract four grey scale levels (the amount as shown as −4 in FIG. **7**). Accordingly, the gray scale level "20" is corrected by the computing circuit **32** to a gray scale level "16"(20−4=16) which level is provided to the X-driver via the buffer circuit **36**. In this way, corrections are made to the transmissivity/applied voltage characteristics where, as shown in FIG. **3**, they are not uniform for each color.

FIG. **9** shows the affect the correction of the present invention has on the transmissivity/applied voltage characteristics. In this figure, the ordinate indicates transmissivity and the abscissa indicates gray scale level all of R/G/B, the same transmissivity is achieved for the same gray scale level. Thus, it is seen that the problem of the subject invention of effectively correcting the difference in the dependency of the transmissivity/applied voltage for each color has been solved.

In accordance with the subject invention, the difference in the dependency of the transmissivity/applied voltage characteristics for each color can be effectively compensated for. Further, the amount of the adjustment can be varied with the grey scale level for accurate compensation.

With the method of the subject invention, only an additional circuit such as a computing circuit, is needed to effectively correct the differences in the transmissivity/applied voltage characteristics for colors. The above correction is made while avoiding the problems in complexity of control methods in the background art. That is, to implement the subject invention, only a condition determination circuit is needed in the data control circuit. It is not necessary to change the structure of the X-driver or the structure of the cell.

Although, in this embodiment, the gray scale data related to B has been made to match the gray scale data related to R and G by performing a subtraction thereof, it should be self evident to those skilled in the art that an addition of the gray scale data related to Red and Green can be used to match the gray scale data for those colors with the gray scale data related to Blue using the teaching of the present invention. Therefore, it should be understood that many changes can be made in the described embodiment without departing from the spirit and scope of the present invention.

We claim:

1. A liquid crystal color display comprising:

a) a display cell containing a light transmitting medium,

b) driver means connected to said display cell for driving the display cell with sets of grey scale data signals each signal for a different color, and

c) data control means for receiving gray scale data signals related to the setting of a gray scale for the display cell and outputting said gray scale data signals to said driver with a predetermined timing, wherein said data control means includes:

i) computing means for changing the level of the gray scale data signals for at least one color relative to the other colors to a different gray scale level to compensate for a variation in intensity between the colors due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and

ii) buffer means for delaying any uncorrected gray scale signal related to the other colors for the time delay caused by said corrected gray scale data signal being corrected.

2. A liquid crystal color display of claim **1** wherein: said data control means comprises adjusting means for varying the amount of correction accorded to the gray scale data signals for said at least one color.

3. A liquid crystal color display of claim **1** wherein: said adjusting means is for the data control means to simultaneously output the corrected and uncorrected gray scale data signals.

4. A liquid crystal color display of claim **1** wherein: said correction performed by said data control means includes an addition or subtraction of the voltage representing at least one gray scale level for at least one color.

5. A method of gray scale data control for eliminating the effect wavelength dependency of transmissivity of light in a multicolor display cell comprising:

changing the level of gray scale data signals related to at least one of the multicolors supplied to the display cell to create a corrected gray scale data signal with a level different from the inputted gray scale data signal to compensate for differences in transmissivity of the colors that result from wavelength dependence, and synchronizing the output of the gray scale data signals by delaying the output for at least one other of the multicolor by the time taken for correction of said at least one color to simultaneously output the gray scale data of all said multicolors.

6. A gray scale control method of claim **5** wherein said correction includes an adding or subtracting voltage level representations of at least one gray scale of said at least one color.

7. A liquid crystal multicolor display comprising:

a) display cells containing a light transmitting medium,

b) driver circuits connected to said display cells for driving the display cells with sets of gray scale data signals each driver circuit for a different one of the colors,

i) calculation logic in the driver circuit of at least one color for changing the level of the gray scale data signals of said at least one color to a different gray scale level to compensate for color distortion due to wavelength related differences in transmissivity between the colors through the light transmitting medium, and

ii) delay logic in the driver circuit for any other of the colors without the calculation logic in its driver circuit for delaying the gray scale signals for the other of the colors to synchronize the provision of the sets of gray scale data signals by compensating for the delay caused by the calculation logic.

8. The liquid crystal color display of claim **7** wherein said data calculation logic provides adjustments for varying the amount of correction in accordance with the level of the gray scale data signals provided to said calculation logic.

9. The liquid crystal display of claim **8** wherein said at least one color is blue and said any of the other colors are red and green.

10. The liquid crystal display of claim **7** wherein said calculation logic includes a tabular lookup table providing different corrective values at different gray scale levels.

11. A liquid crystal color display of claim **10** wherein said correction performed by said data control means includes an addition or subtraction of the binary signal representing a change of at least one gray scale level for at least one color.

12. A method of gray scale data control for reducing the effect wavelength dependency on transmissivity of light in cells of a multicolor display comprising:

changing the gray scale data signals related to one of the multicolors to correct for the wavelength dependency of transmissivity and thereby create a corrected gray scale data signal different from the inputted gray scale data signal for that color, and synchronizing the timing of the gray scale data signals by delaying the output for any other color of the multicolors with gray scale data signals not subject to a correction by the amount of time taken for correction of the one color to synchronize the timing of the gray scale data signals for all said multicolors.

13. The method of claim **12** including varying the magnitude of the corrective change as a function of the gray scale level of said one of the multicolors.

* * * * *

EXHIBIT E

US006013923A

United States Patent [19]

Huang

[11] Patent Number: 6,013,923

[45] Date of Patent: Jan. 11, 2000

[54] **SEMICONDUCTOR SWITCH ARRAY WITH ELECTROSTATIC DISCHARGE PROTECTION AND METHOD OF FABRICATING**

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[73] Assignee: **1294339 Ontario, Inc.**, Toronto, Canada

[21] Appl. No.: **09/000,479**

[22] PCT Filed: **Jul. 31, 1995**

[86] PCT No.: **PCT/CA95/00454**

§ 371 Date: **Jul. 21, 1998**

§ 102(e) Date: **Jul. 21, 1998**

[87] PCT Pub. No.: **WO97/05654**

PCT Pub. Date: **Feb. 13, 1997**

[51] **Int. Cl.**[7] **H01L 23/62**

[52] **U.S. Cl.** **257/59**; 257/356

[58] **Field of Search** 349/139, 143; 257/59, 355–363

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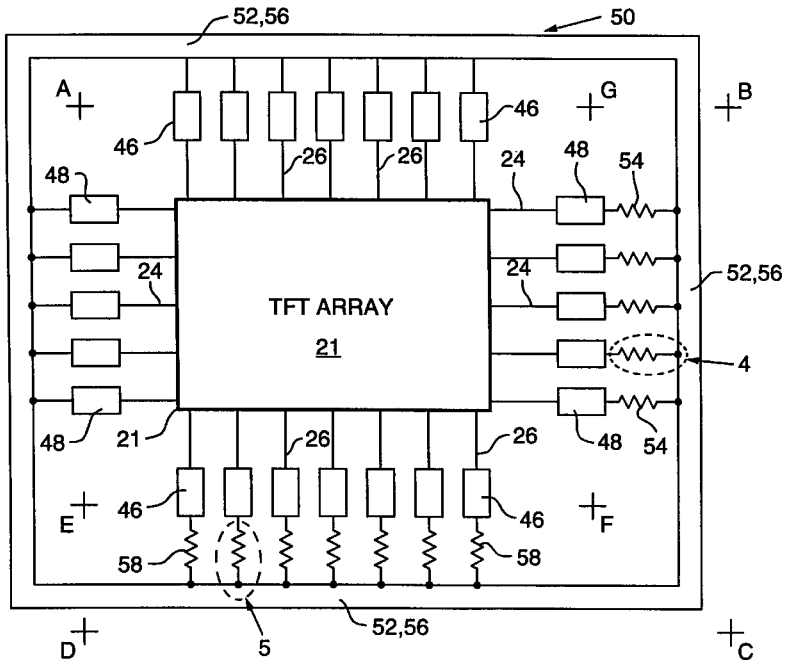
Primary Examiner—David B. Hardy

Attorney, Agent, or Firm—Fay, Sharpe, Fagan, Minnich & McKee, LLP

[57] **ABSTRACT**

A method of inhibiting electrostatic discharge damage to an array of semiconductor switches **(21)** formed on a common substrate and arranged in rows and columns comprises the steps of: during formation of gate lines **(24)** that interconnect one of the rows and columns of the array, connecting one end of each gate line directly to a shorting ring **(52)** and another end of each gate line to a shorting ring **(56)** via a protection element **(54)**; during formation of the source lines **(26)** that interconnect the other of the rows or columns of the array, connecting one end of each source line directly to a shorting ring **(56)** and connecting another end of each source line to a shorting ring **(56)** via a protection element **(58)**; and electrically coupling the shorting rings **(52, 56)**. A semiconductor switch array **(21)** incorporating electrostatic discharge protection **(50)** is also provided.

20 Claims, 7 Drawing Sheets



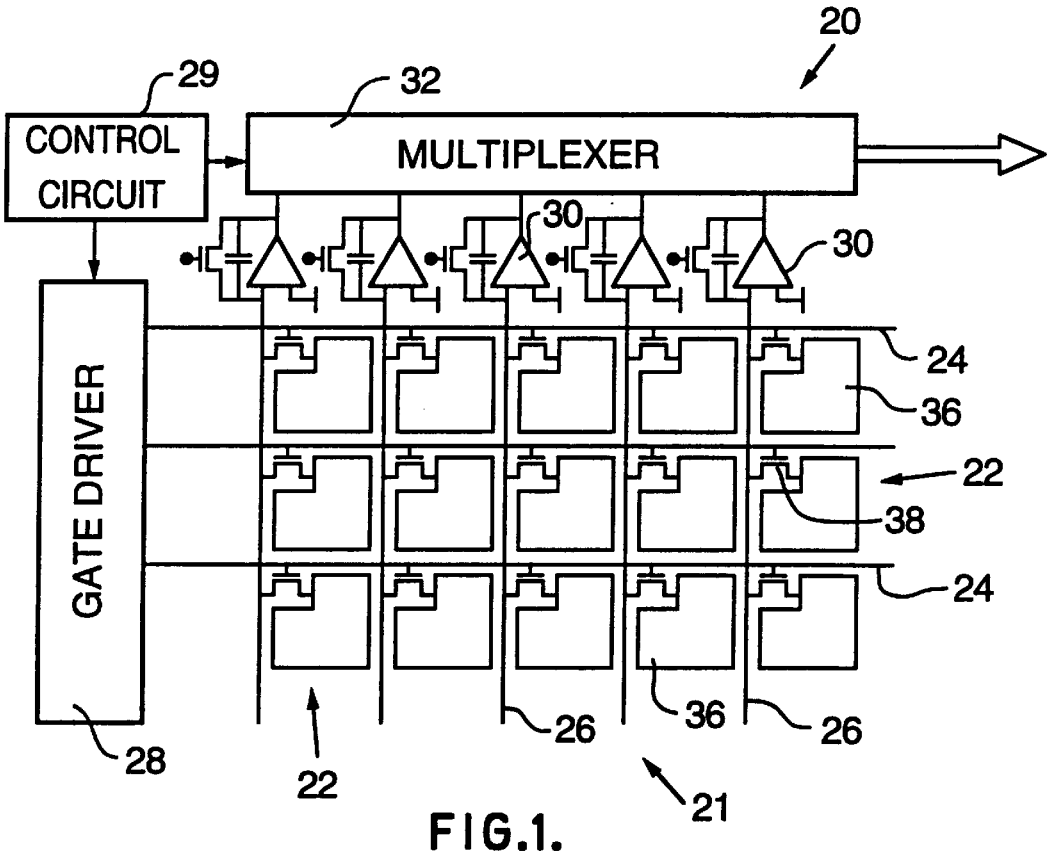

20
29
32
CONTROL CIRCUIT
MULTIPLEXER
30
30
24
36
22
38
24
GATE DRIVER
26
36
26
28
22
21

FIG.1.

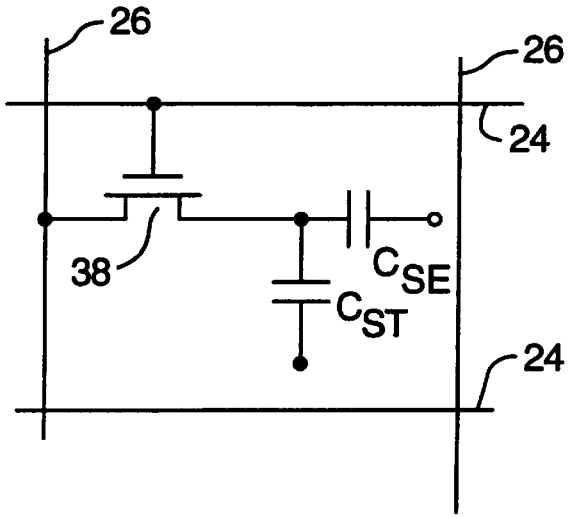

26
26
24
38
C_{SE}
C_{ST}
24

FIG.2.

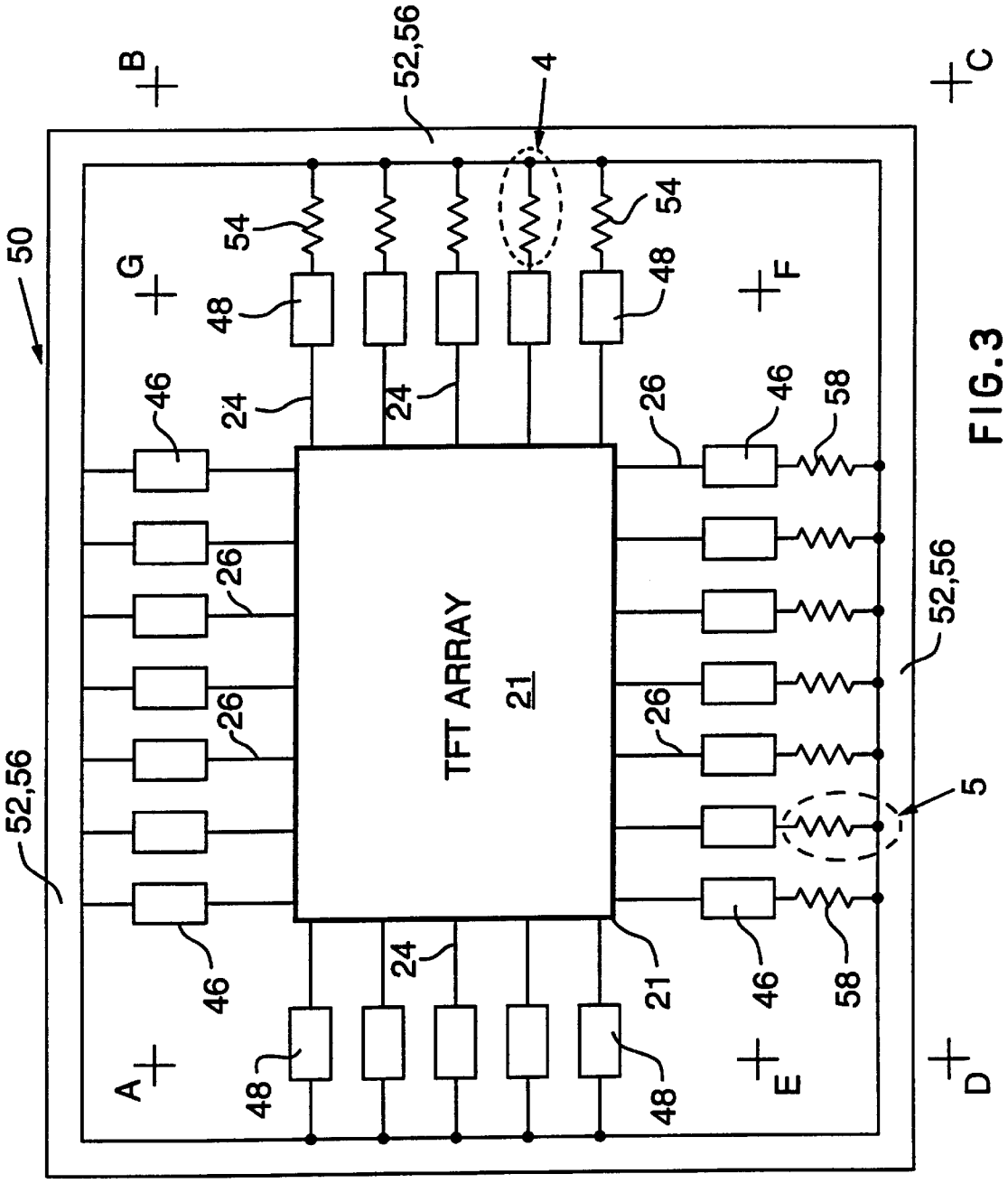

B
52,56
4
C
50
G
54
48
F
54
48
46
24
24
26
46
58
TFT ARRAY
21
26
52,56
26
26
5
52,56
46
24
21
46
58
A
48
48
E
D

FIG.3

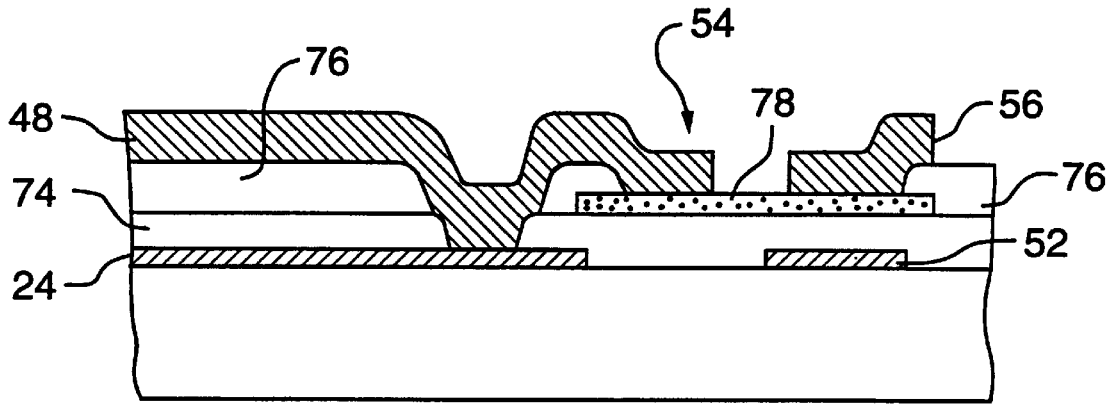


FIG.4

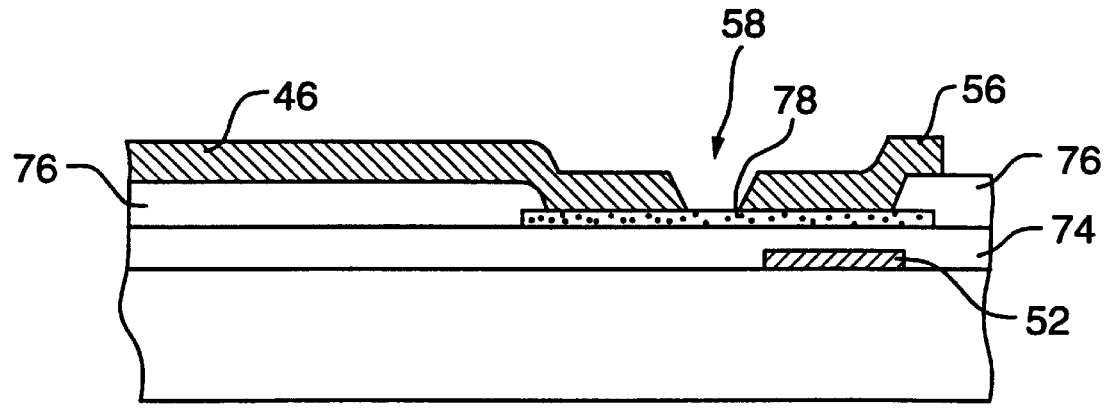


FIG.5

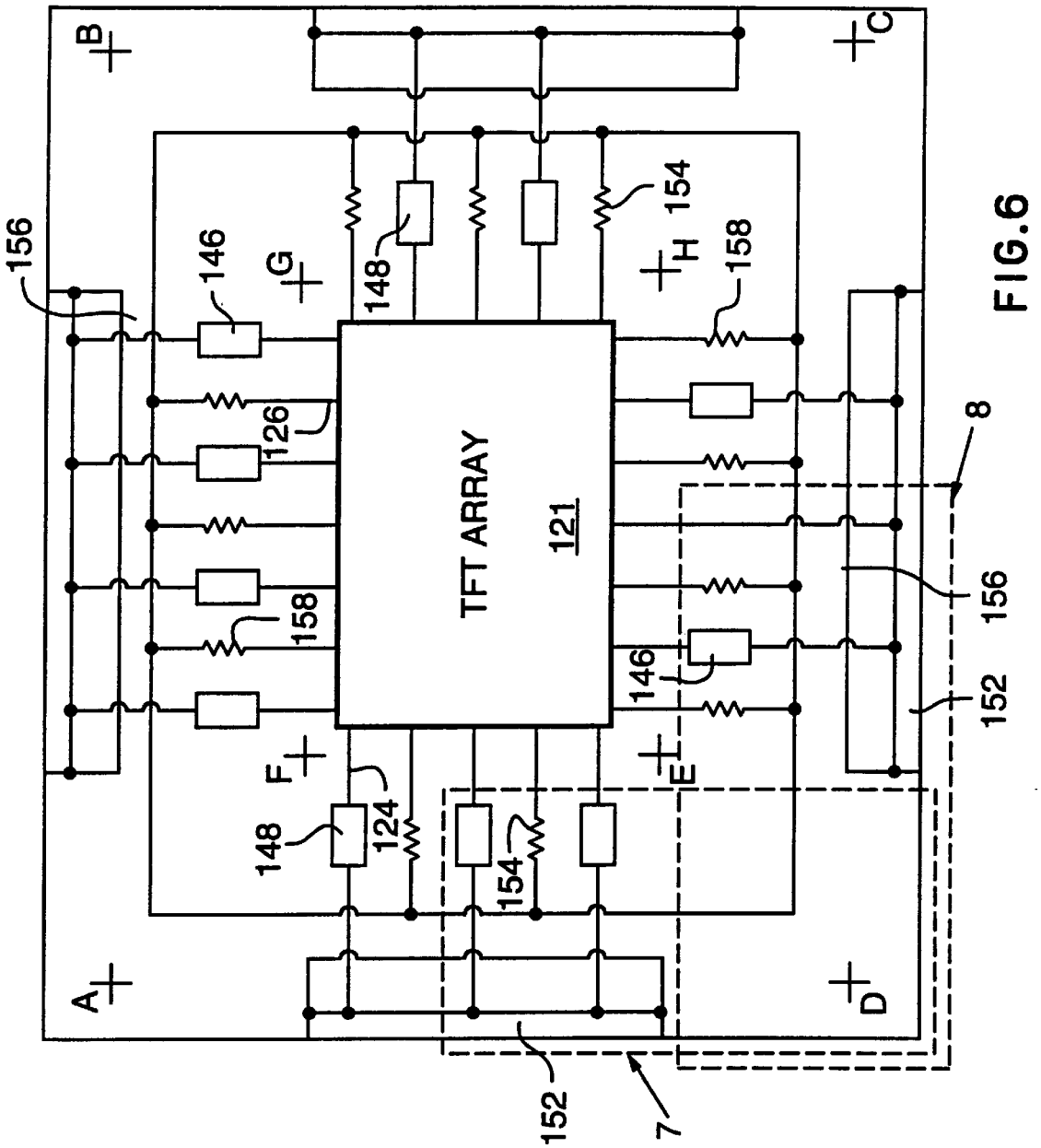


FIG.6

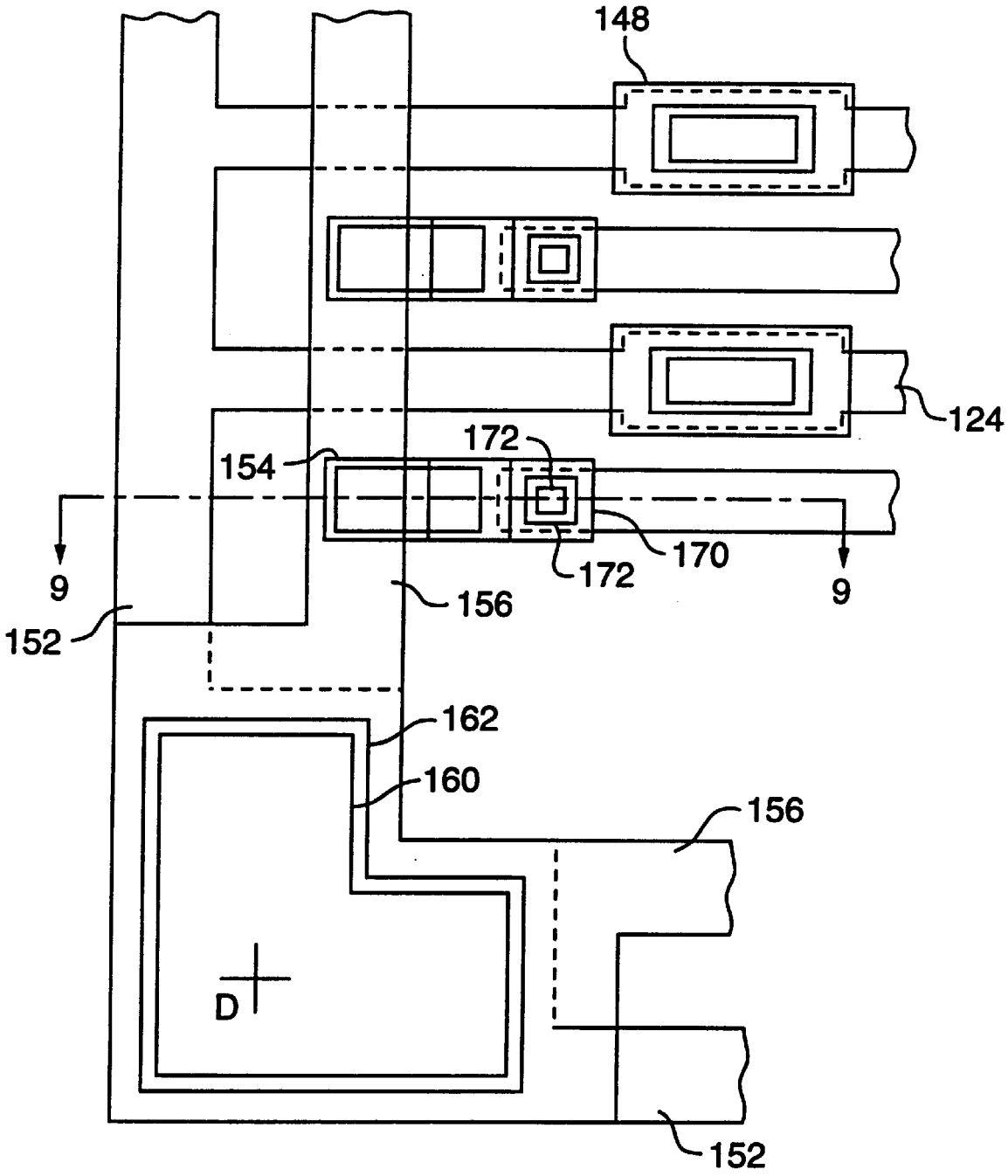


FIG.7

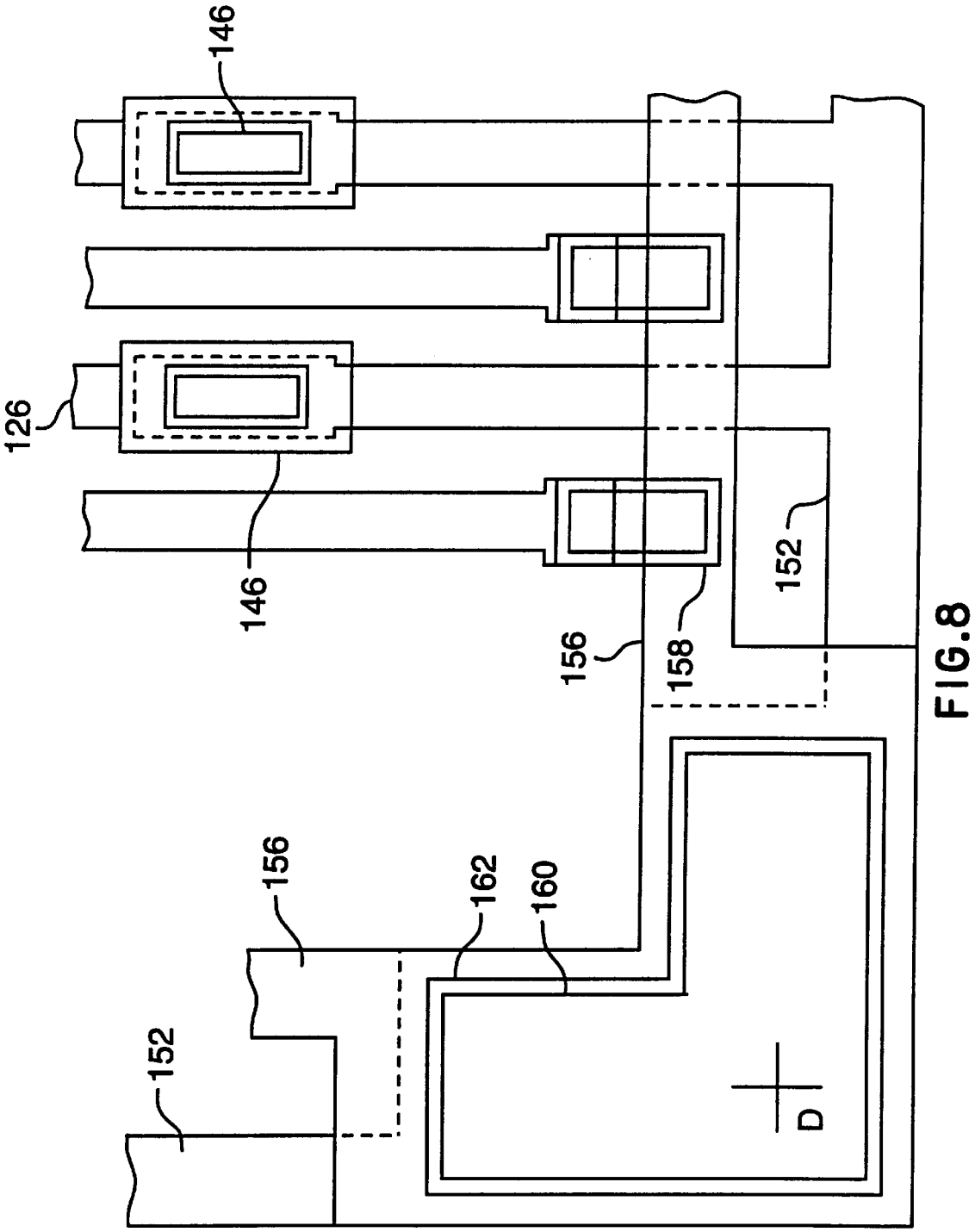


FIG.8

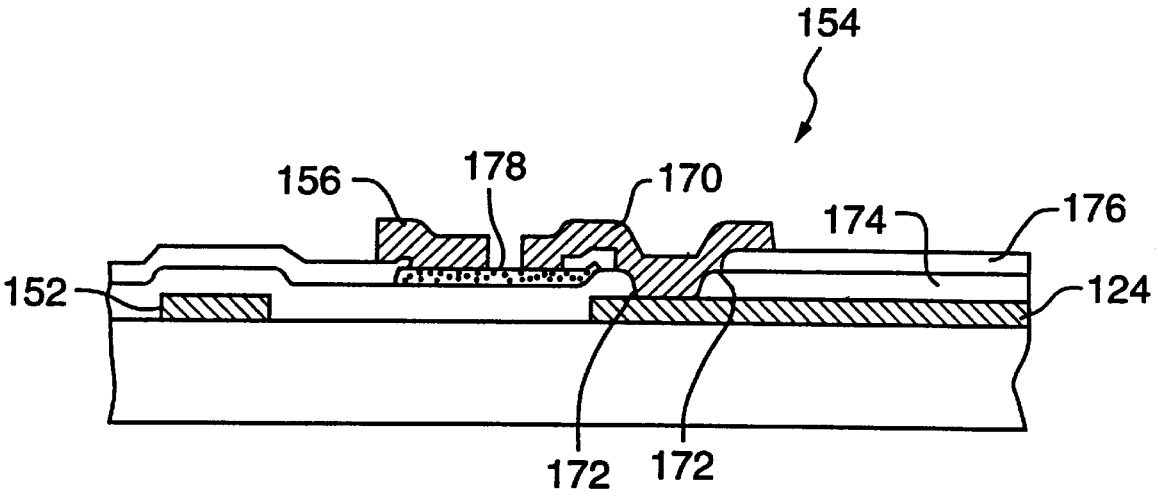


FIG.9

SEMICONDUCTOR SWITCH ARRAY WITH ELECTROSTATIC DISCHARGE PROTECTION AND METHOD OF FABRICATING

TECHNICAL FIELD

The present invention relates to a method of protecting a semiconductor switch array from electrostatic discharge damage and to a semiconductor switch array incorporating electrostatic discharge protection.

BACKGROUND ART

Electrostatic discharge (ESD) damage is a well known phenomenon and can occur during the fabrication of semiconductor devices such as metal-oxide semiconductor (MOS) structures. In structures of this nature, ESD damage can result in gate insulating layer breakdown, large shifts in threshold voltage and large leakage currents between the gate and source electrodes or gate and drain electrodes.

ESD damage is a more pronounced problem during the fabrication of thin film transistor (TFT) switch arrays for use in liquid crystal displays or in flat panel detectors for radiation imaging. This is due to the fact that the TFT switches are formed on an insulating substrate (typically glass) and thus, the source and drain electrodes may charge to a very high voltage. Also, because peripheral circuits to which the TFT switch array is to be connected are generally not formed on the same substrate as the TFT switch array, the gate and source lines must extend from the TFT switch array sufficiently to allow the peripheral circuits to be connected to the TFT switch array via wire bonding pads. Any static charge picked up by the gate and source lines is transferred to the gate and source electrodes of the TFT switches as well as to the intersecting nodes of the gate and source lines where the static charge is held. If the static charge reaches a high enough level, the dielectric gate insulating layer between the gate and source electrodes may breakdown. Even if this breakdown can be avoided, the voltage differential between the gate and source electrodes or gate and drain electrodes caused by this held static charge may cause the threshold voltage of the TFT switches to shift in either a positive or negative direction.

Recently, a large amount of attention has been given to the problems resulting from ESD damage especially in active matrix liquid crystal displays and flat panel detectors for radiation imaging. It is now believed that ESD damage is also caused by equipment related problems during the fabrication, handling and testing of these types of devices. The trends to use higher throughput equipment with higher speed substrate handling as well as to downscale during the fabrication process to reduce metal line width and reduce parasitic capacitance in the TFT switches decrease ESD immunity.

One common ESD damage protection circuit used with TFT switch arrays makes use of closed shorting bars surrounding the TFT switch array to link all of the source lines and the gate lines of the TFT switch array together. The shorting bar associated with the gate lines is formed at the time the gate lines are formed while the shorting bar associated with the source lines is formed at the time the source lines are formed. The two shorting bars are electrically connected through vias formed in the TFT switch array structure. Because the shorting bars connect the gate and source electrodes of all of the TFT switches in the array, the gate and source electrodes remain at the same potential throughout the fabrication process. This prevents any voltage differentials from occurring across the gate and source electrodes and therefore, inhibits ESD damage at these electrodes.

Once the TFT switch array has been completely fabricated, the shorting bars are removed by cutting off part of the glass substrate where the shorting bars located. This cutting process is done before the individual TFT switches are tested and before the gate and source lines are connected to peripheral circuits.

Although the above ESD damage protection circuit is widely used, once the shorting bars have been removed, to ESD damage protection remains. This poses problems since ESD damage often occurs during testing of the TFT switches and during bonding of the gate and source lines to peripheral equipment. This is in view of the fact that at this stage, the TFT switch array is handled by individuals and contacted with electronic measuring equipment.

Another ESD damage protection network for TFT switch arrays is disclosed in U.S. Pat. No. 4,803,536. This ESD damage protection network makes use of a strip of N^+ amorphous silicon resistive material film extending to all of the bonding pads. The value of the resistive material film is at least an order of magnitude greater than the impedance of external driver circuits connected to the bonding pads. By manipulating the resistance of the resistive material film, static charges disperse to all of the gate and source lines with an RC constant. Although individual TFT switches can be tested without removing the resistive material film, the resistive material film crosses over all of the gate and source lines. This causes crosstalk and electronic noise which in certain applications, such as x-ray imaging where signal currents are small, are serious problems.

U.S. Pat. No. 5,313,319 discloses yet another ESD protection circuit for a TFT switch array. This protection circuit includes static protection capacitors formed on the substrate of the TFT switch array between the gate and source lines. The thickness of the static protection capacitors are chosen to ensure that they breakdown due to static charges before ESD damage to the TFT switches occurs. Unfortunately, the static protection capacitors increase stray capacitance in the TFT switch array thereby increasing electronic noise making the TFT switch array unsuitable for many applications.

Japanese Patent Nos. JPA2-61618, JPA62-198826 and JPA1-303416 and U.S. Pat. No. 5,371,351 disclose an ESD protection circuit for a TFT switch array which makes use of photodiodes formed of an a-Si film. The photodiodes connect the gate lines with the source lines to minimize any potential voltage difference between them. When the photodiodes are illuminated, the resistance of the protection circuit decreases dramatically creating short circuits between the gate and source lines. When testing individual TFT switches, or when operating the TFT switch array in normal conditions, no incident light is permitted to impinge on the photodiodes. This keeps the resistance of the protection circuit very high to minimize crosstalk and leakage currents.

U.S. Pat. No. 5,220,443 discloses an ESD protection circuit for a TFT switch array. The protection circuit includes a common electrode interconnecting the gate and source lines. Non-linear resistive elements having a resistance that decreases with an increase in voltage are connected between the gate and source lines. The non-linear resistive elements are realized using two back to back thin film diodes. Because the resistive elements provide a large resistance between the gate and source lines, individual TFT switches can be tested without cutting the glass substrate.

Even after cutting the glass substrate, some of the non-linear resistive elements remain to improve the immunity of the TFT switch array to ESD damage. However, the immunity of the TFT switch array to ESD damage after cutting is significantly less than before cutting.

The prior art ESD protection circuits referred to above all have some common drawbacks. Firstly, none of the ESD protection circuits protect the TFT switch array from the first manufacturing stage (usually gate line formation) to the last manufacturing stage (usually wire bonding). During the manufacture of TFT switch arrays for liquid crystal displays, it has been found that ESD damage may occur during the process of spin coating or stripping photoresist, during the cleaning process using DI water, and during plasma etching. These processes are often performed prior to the completion of the TFT switch array structure. Isolating the gate lines before finishing source line metallization as suggested in the prior art may result in the build up of electrostatic charge on the gate lines. Electrostatic charges on the gate lines may become buried under the dielectric film forming the gate insulating layer and incubate until later stages in the manufacturing process. During these later stages, the buried electrostatic charges may move along the gate lines and concentrate at a few points or boundary lines causing a breakdown in the dielectric gate insulating layer.

In addition, in some instances since the gate and source lines are interconnected by protection elements, a failure in the connection between a gate or source line and a protection element will result in the gate or source line being isolated from the common electrode.

In the case of U.S. Pat. No. 5,220,443, although some ESD damage protection circuitry remains on the substrate during the wire bonding process, the impedance between an arbitrary gate line and a source line may become too large to discharge electrostatic charge quickly enough to avoid ESD damage. Accordingly, better protection against ESD damage is desired.

It is therefore an object of the present invention to provide a reliable method of protecting a semiconductor switch array from ESD damage and a semiconductor switch array incorporating electrostatic discharge protection which obviates or mitigates at least one of the above-described disadvantages.

SUMMARY OF THE INVENTION

According to one aspect of the present invention there is provided a method of inhibiting electrostatic discharge damage to an array of semiconductor switches formed on a common substrate and arranged in rows and columns, individual ones of one of the rows or columns of said array being interconnected by source lines and the individual ones of the other of the rows or columns of said array being interconnected by gate lines, said method comprising the steps of:

during formation of said gate lines, connecting one end of each gate line directly to a shorting element and another end of each gate line to a shorting element via a protection element;

during formation of said source lines, connecting one end of each source line directly to a shorting element and connecting another end of each source line to a shorting element via a protection element; and

electrically coupling said shorting elements.

According to yet another aspect of the present invention there is provided a semiconductor switch array incorporating electrostatic discharge protection comprising:

an array of semiconductor switches formed on a common substrate and arranged in rows and columns, the individual ones of one of the rows or columns of said array being interconnected by source lines and the individual ones of the other of said rows or columns being interconnected by gate lines; and

a pair of electrically coupled shorting elements formed on said substrate, each of said gate and source lines being connected to one of said shorting elements directly and to one of said shorting elements via a protection element.

In one embodiment, it is preferred that the method further comprises the step of connecting the one and another ends of each of the source lines to a first shorting element, connecting the one ends of each of the gate lines to a second shorting element and the another ends of each of the gate lines to the first shorting element electrically coupling the first and second shorting elements.

In another embodiment, it is preferred that the method further comprises the step of connecting the one ends of the source and gate lines to a first shorting element, connecting the another ends of the source and gate lines to a second shorting element and electrically coupling the first and second shorting elements. In this case, it is also preferred that the one and another ends of the source and gate lines alternate between opposite sides of the array. In both embodiments, it is preferred that the protection elements are in the form of resistive protection elements.

The present invention provides advantages in that the ESD damage protection is maintained throughout the entire manufacturing and testing process of the semiconductor switch array and is fully compatible with conventional semiconductor switch array fabrication processes.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the present invention will now be described more fully with reference to the accompanying drawings in which:

FIG. **1** is a schematic of a flat panel detector for radiation imaging incorporating a TFT switch array;

FIG. **2** is an equivalent circuit of a pixel forming part of the flat panel detector illustrated in FIG. **1**;

FIG. **3** is a schematic of a TFT switch array incorporating an ESD damage protection circuit;

FIG. **4** is a cross-sectional view of FIG. **3**;

FIG. **5** is another cross-sectional view of FIG. **3**;

FIG. **6** is a schematic of an alternative embodiment of a TFT switch array incorporating an ESD damage protection circuit;

FIG. **7** is a top plan view of a portion of the TFT switch array illustrated in FIG. **6**;

FIG. **8** is a top plan view of another portion of the TFT switch array illustrated in FIG. **6**; and

FIG. **9** is a cross-sectional view of FIG. **7** taken along line **9—9**.

BEST MODES FOR CARRYING OUT THE INVENTION

Referring now to FIG. **1**, a flat panel detector for radiation imaging is shown and is generally indicated by reference numeral **20**. The flat panel detector includes a semiconductor switch array **21** in the form of a plurality of pixels **22** arranged in rows and columns. Gate lines **24** interconnect the pixels **22** of each row while source lines **26** interconnect the pixels of each column. The gate lines **24** lead to a gate driver circuit **28** which provides pulses to the gate lines in

succession in response to input from a control circuit **29**. The source lines **26** lead to charge amplifiers **30** which in turn are connected to an analog multiplexer **32**. The analog multiplexer provides image output which can be digitized to create a digitized radiation image in response to input from the control circuit **29**.

FIG. **2** shows an equivalent circuit of one of the pixels **22**. As can be seen, the pixel **22** includes a radiation transducer CS. coupled to a storage capacitor C_{ST} in the form of a pixel electrode **36**. The pixel electrode **36** constitutes the drain electrode of a thin film transistor ("TFT") switch **38**. The source electrode of TFT switch **38** is coupled to one of the source lines **26** while the gate electrode of the TFT switch is coupled to one of the gate lines **24**.

When the radiation transducer C_{SE} is biased and is exposed to radiation, it causes the pixel electrode to store a charge proportional to the exposure of the radiation transducer C_{SE}, to radiation. Once charged, the charge can be read by supplying a gating pulse to the gate terminal of TFT switch **38**. When the TFT switch receives the gate pulse, it connects the pixel electrode **36** to the source line **26** allowing the pixel electrode to discharge. The charge on the source line **26** is detected by the charge amplifier **30** which in turn generates an output voltage proportional to the detected charge. The output voltage of the charge amplifier is conveyed to the analog multiplexer **32**.

Referring now to FIG. **3**, during the fabrication process, the array **21** of pixels **22** including the gate and source lines **24** and **26** respectively are fabricated on a common glass substrate. Wire bonding pads **46** are formed at the ends of the source lines **26** for testing or for wire bonding purposes. Similarly, wire bonding pads **48** are formed at the ends of the gate lines **24**. As mentioned previously, during fabrication of the TFT switch array **21**, during its testing or when connecting peripheral circuits to the TFT switch array **21** such as gate driver **28** and charge amplifiers **30**, ESD damage to the TFT switch array may occur. To reduce the occurence of ESD damage during fabrication of the TFT switch array **21**, an ESD damage protection circuit **50** is also fabricated on the glass substrate as will now be described.

The ESD damage protection circuit **50** includes a first shorting element in the form of a ring **52** surrounding the TFT switch array and interconnecting all of the gate lines **24** of the TFT switch array **21**. Specifically, the shorting ring **52** is connected directly to the wire bonding pads **48** on one side of the TFT switch array **21**.

A second shorting element in the form of a ring **56** also surrounds the TFT switch array and interconnects all of the source lines **26** of the TFT switch array **21**. The second shorting ring **56** is connected directly to the wire bonding pads **46** on one side of the TFT switch array **21** and is connected to the wire bonding pads **46** on the other side of the TFT switch array through resistive protection elements **58**. Shorting ring **56** is also connected to each of the wire bonding pads **48** on the other side of the TFT switch array **21** through a resistive protection element **54**. The two shorting rings **52** and **56** are electrically connected through vias (not shown) formed in the TFT switch array structure. The resistive protection elements **54**, **58** provide current paths for leaking electrostatic charges collected by the gate and source lines **24** and **26** and have resistances at least one order of magnitude greater than the impedance of the gate and source lines.

FIGS. **4** and **5** best illustrate the resistive protection elements **54** and **58** respectively. As can be seen in FIG. **4**, resistive protection element **54** includes a Cadmium Selenide (CdSe) semiconductor material channel **78**. Wire bonding pad **48** contacts the channel **78** through a via formed in the gate insulating layer **74** and passivation layer **76**. Shorting ring **56** also contacts the channel **78**. Resistive protection element **58** also includes a CdSe channel **78** contacted by wire bonding pad **46** and shorting ring **56**. Shorting ring **56** as mentioned previously is connected to shorting ring **52** through vias (not shown). The resistances of the resistive protection elements **54** and **58** can be designed to change with bias voltage in a linear or non-linear manner and may take the form of one of a variety of structures such as for example, TFT switches, TFD's (thin film diodes), zener diodes or photodiodes.

As one of skill in the art will appreciate, the shorting ring **52** is formed when the gate lines **24** are being formed on the substrate of the TFT switch array structure. The shorting ring **56** is formed when the source lines **26** are being formed on the substrate.

After the TFT switch array **21** and ESD damage protection circuit **50** have been formed on the glass substrate, the TFT switch array structure can be cut along scribe lines ABCDA to expose the wire bonding pads **46** and **48** connected to the source and gate lines extending from one side of the TFT switch array permitting the individual TFT switches **38** in the array to be tested. These scribe lines are marked so that part of each shorting ring **52**, **56** remains intact keeping the gate and source lines **24** and **26** interconnected through the resistive protection elements **54** and **58** during the testing stage. If electrostatic charges appear on the gate or source lines resulting in any unbalanced potentials across the dielectric film constituting the gate insulating layer of the TFT switch array, the electrostatic charges will disperse quickly through the resistive protection elements connected to the gate and source lines.

Once testing has been completed, the outputs from the gate driver **28** can be connected to the wire bonding pads **48** of the exposed gate lines **24** via a wire bonding process. Similarly, the inputs to the charge amplifiers **30** can be connected to the wire bonding pads **46** of the exposed source lines **26** via a wire bonding process. Thus, the TFT switch array **21** can be connected to the peripheral circuitry with half of the ESD damage protection circuit intact.

After the wire bonding processes have been completed, the remaining half of the ESD damage protection circuit **50** can be severed from the TFT switch array **21** using a laser cutting operation made along scribe lines EFG. However, the remaining half of the ESD damage protection circuit may be useful when the flat panel detector **20** is in operation by allowing gate pulses applied to the gate lines to be fed back to the gate driver **28** to shape the gate pulse waveform or to reduce electronic noise. In addition, the remaining connections between the resistive protection elements **54** and **58** and the shorting rings **52** and **56** permits excess charge to leak to ground, in the event that bond-wires peel off or in the event that defects in the charge amplifiers **30** or gate drivers **28** occur.

In some applications especially in high resolution TFT liquid crystal displays and TFT flat panel detectors, it is desired to use peripheral circuitry connected to the gate and source lines on both sides of the TFT switch array **21**. Referring now to FIGS. **6** to **9**, another embodiment of a TFT switch array **121** incorporating an ESD damage protection circuit **150** is shown which is better suited to accommodate double-sided peripheral circuitry. In this embodiment, like reference numerals will be used to indicate like components with a ("100") added for clarity.

As can be seen, the ESD damage protection circuit **150** includes a shorting ring **152** interconnecting all of the gate lines **124** of the TFT switch array **121**. The shorting ring **152** is connected to only one end of each gate line **124** through wire bonding pads **148**. The connections between the shorting ring **152** and the wire bonding pads **148** alternate between opposite sides of the TFT switch array. Shorting ring **152** also interconnects all of the source lines **126** of the TFT switch array through vias formed in the TFT switch array structure. The shorting ring **152** is connected to only one end of each source line **126** through wire bonding pads **146**. The connections between the shorting ring **152** and the wire bonding pads **146** also alternate between opposite sides of the TFT switch array **121**.

A second shorting ring **156** is connected to the other end of each gate line **124** via resistive protection elements **154**. Shorting ring **156** is also connected to the other end of each source line **126** via resistive protection elements **158**. The shorting rings **152** and **156** are electrically connected through vias **160** and **162** formed at the corners of the TFT switch array structure (see FIGS. **7** and **8**).

FIG. **7** best illustrates one of the resistive protection elements **154** although it should be realized that both sets of resistive protection elements **154** and **158** are similar. As can be seen, resistive protection element **154** includes a metal connection tab **170** contacting gate line **124** through vias **172** formed in the gate insulating and passivation layers **174** and **176** of the TFT switch array structure. The tab **170** contacts a CdSe semiconductor material channel **178**. The shorting ring **156** also contacts the channel **178** but is spaced from the connection tab **170**.

After the TFT switch array **121** and ESD protection circuit **150** have been formed on the glass substrate, the TFT switch array can be cut along scribe lines ABCDA to permit the individual TFT switches in the TFT switch array to be tested. Similar to the previous embodiment, the scribe lines are marked so that after cutting, one end of each of the gate and source lines **124** and **126** remains connected to shorting ring **156** via resistive protection elements **154** and **158** respectively.

Once testing has been completed, the peripheral circuits can be connected to the exposed wire bonding pads **146** and **148** on opposite sides of the TFT switch array **121**. After this, the connections between the gate and source lines and the shorting ring **156** can be severed using a programmable laser cutting machine programmed to jump over the gate and source lines **124** and **126** connected to peripheral circuits.

As one of skill in the art will appreciate, the ESD damage protection circuits are present from the first manufacturing stage of the TFT switch array (gate line formation) right through to testing and connection of the TFT switch array to peripheral circuits. Because of this, the likelihood of ESD damage occurring to the TFT switch array is reduced as compared to prior art switch arrays.

Although the ESD damage protection circuits have been described in conjunction with a TFT switch array used in a flat panel detector for radiation imaging, it should be apparent to those of skill in the art that the ESD damage protection circuits can be fabricated during the formation of TFT switch arrays for other applications. Also, the ESD damage protection circuits can be fabricated during the formation of other semiconductor switch arrays where it is desired to protect the switch array from ESD damage during its formation and testing.

Those of skill in the art will also appreciate that variations and modifications may be made to the present invention without departing from the scope thereof as defined by the appended claims.

What is claimed is:

1. A method of inhibiting electrostatic discharge damage to an array of semiconductor switches formed on a common substrate and arranged in rows and columns, individual ones of one of the rows or columns of said array being interconnected by source lines and individual ones of the other of the rows or columns of said array being interconnected by gate lines, said method comprising the steps of:

during formation of said gate lines, connecting one end of each gate line directly to a shorting element and another end of each gate line to a shorting element via a protection element;

during formation of said source lines, connecting one end of each source line directly to a shorting element and connecting another end of each source line to a shorting element via a protection element; and

electrically coupling said shorting elements.

2. The method of claim **1** further comprising the steps of connecting said one and another ends of each of said source lines to a first shorting element, connecting said one end of each of said gate lines to a second shorting element and said another end of each of said gate lines to said first shorting element and electrically coupling said first and second shorting elements.

3. The method of claim **2** wherein said protection elements are in the form of resistive protection elements.

4. The method of claim **3** wherein the one ends of each source line extend from one side of said array and said another ends of each source line extend from an opposite side of said array and wherein the one ends of each gate line extend from one side of said array and said another ends of each gate line extend from an opposite side of said array.

5. The method of claim **3** further comprising the step of initially cutting said array along a first set of scribe lines to expose the one ends of said gate and source lines while maintaining the electrical connection between the first and second shorting elements and the another ends of said gate and source lines.

6. The method of claim **5** further comprising the step of further cutting said array along a second set of scribe lines to sever the connection between said another ends of said gate and source lines and said protection elements.

7. The method of claim **6** wherein said further cutting is performed using a laser cutting operation.

8. The method of claim **1** further comprising the step of connecting said one ends of said source and gate lines to a first shorting element, connecting said another ends of said source and gate lines to a second shorting element and electrically coupling said first and second shorting elements.

9. The method of claim **8** wherein said one and another ends of said source and gate lines alternate between opposite sides of said array.

10. The method of claim **9** wherein said protection elements are in the form of resistive protection elements.

11. The method of claim **10** further comprising the step of initially cutting said array along a first set of scribe lines to expose the one ends of said gate and source lines while maintaining the electrical connection between the first and second shorting elements and the another ends of said gate and source lines.

12. The method of claim **11** further comprising the step of further cutting said array along a second set of scribe lines to sever the connection between said another ends of said gate and source lines and said protection elements.

13. The method of claim **12** wherein said further cutting is performed using a laser cutting operation.

14. A semiconductor switch array incorporating electrostatic discharge protection comprising:

an array of semiconductor switches formed on a common substrate and arranged in rows and columns, the individual ones of one of the rows or columns of said array being interconnected by source lines and the individual ones of the other of said rows or columns being interconnected by gate lines; and

a pair of electrically coupled shorting elements formed on said substrate, each of said gate and source lines being connected to one of said shorting elements directly and to one of said shorting elements via a protection element.

15. A semiconductor switch array as defined in claim **14** wherein said protection elements are in the form of resistive protection elements.

16. A semiconductor switch array as defined in claim **15** wherein one end of each source line is connected directly to one of said shorting elements and the other end of each source line is connected to said one shorting element via said protection element and wherein one end of each gate line is connected directly to another of said shorting elements and the other end of each gate line is connected to said one shorting element via said protection element.

17. A semiconductor switch array as defined in claim **16** further including scribe lines to guide cutting thereof to expose said one ends of said gate and source lines while maintaining the electrical connection of said other ends of said gate and source lines to said one and another shorting elements.

18. A semiconductor switch array as defined in claim **15** wherein one end of each of said source and gate lines is connected directly to one of said shorting elements and wherein the other end of each of said source and gate lines is connected to another of said shorting elements via a protection element.

19. A semiconductor switch array as defined in claim **18** wherein said one and other ends of said gate and source lines alternate between opposite sides of said array.

20. A semiconductor switch array as defined in claim **19** further including scribe lines to guide cutting thereof to expose said one ends of said gate and source lines while maintaining the electrical connection of said other ends of said gate and source lines to said another shorting element.

* * * * *

EXHIBIT F

US005619352A

United States Patent [19]

Koch et al.

[11] Patent Number: 5,619,352

[45] Date of Patent: Apr. 8, 1997

[54] **LCD SPLAY/TWIST COMPENSATOR HAVING VARYING TILT AND /OR AZIMUTHAL ANGLES FOR IMPROVED GRAY SCALE PERFORMANCE**

[75] Inventors: **Gene C. Koch**, Swisher, Iowa; **Bruce K. Winker**, Moorpark; **William J. Gunning, III**, Newbury Park, both of Calif.

[73] Assignee: **Rockwell International Corporation**, Seal Beach, Calif.

[21] Appl. No.: **690,033**

[22] Filed: **Jul. 31, 1996**

Related U.S. Application Data

[63] Continuation of Ser. No. 313,476, Sep. 30, 1994, abandoned, which is a continuation-in-part of Ser. No. 223,251, Apr. 4, 1994, Pat. No. 5,504,603.

[51] **Int. Cl.**[6] **G02F 1/1333**; G02F 1/1335; G02F 1/13

[52] **U.S. Cl.** **349/89**; 349/117; 349/119; 349/177

[58] **Field of Search** 359/73, 53, 93, 359/102, 51, 52, 63, 499

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Primary Examiner—William L. Sikes
Assistant Examiner—Walter J. Malinowski
Attorney, Agent, or Firm—Gregory G. Williams; M. Lee Murrah; George A. Montanye

[57] **ABSTRACT**

A twisted/splayed O-plate compensation device, in accordance with the invention, is comprised of an organic liquid crystal polymer thin film and possibly one or more other birefringent layers. The O-plate thin film is a birefringent medium with its optical symmetry axis, on average, oriented obliquely with the surface of the film. Within this constraint, the direction of the material's optical symmetry axis is allowed to vary continuously along the axis normal to the film surface. Such films may be fabricated by applying thin layers of chiral doped nematic or semectic liquid crystal monomer solutions in inert solvents to transparent substrates. The carrier solvents are then evaporated and the monomers polymerized by UV irradiation. Compensation devices may also be comprised of multiple layers of twisted/splayed O-plate material in conjunction with A-plates, C-plates, and simple O-plates. Fabrication techniques for twisted/splayed O-plates are described.

29 Claims, 13 Drawing Sheets

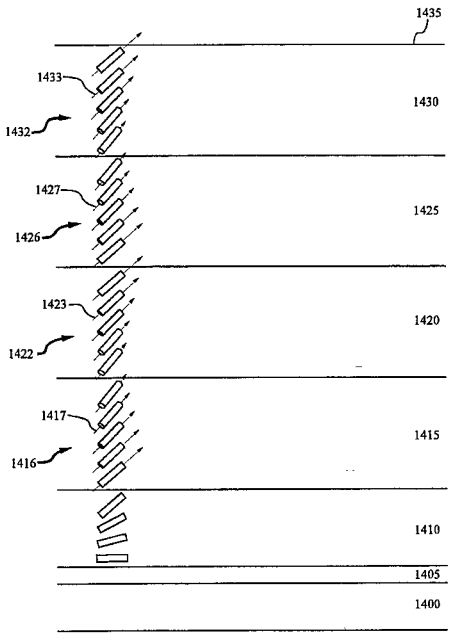


Figure 1A
(Prior Art)

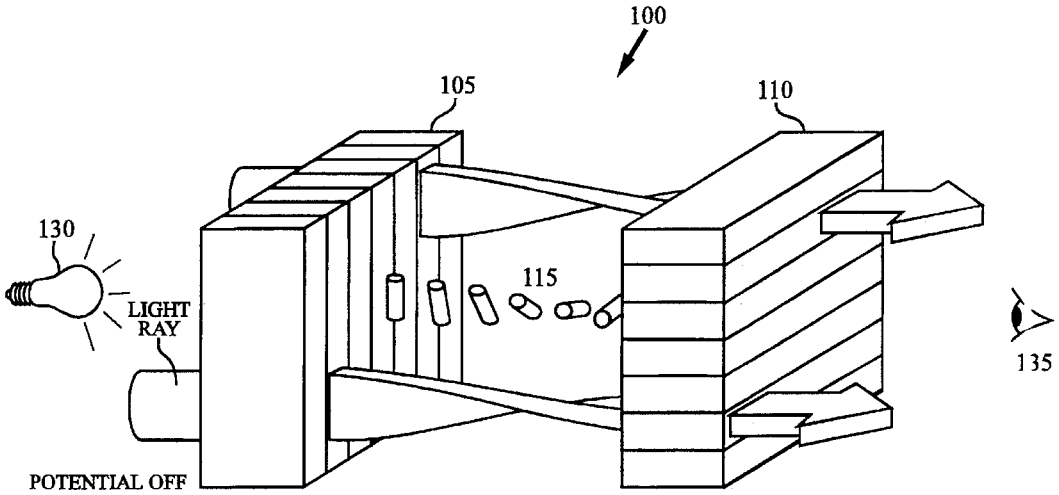


Figure 1B
(Prior Art)

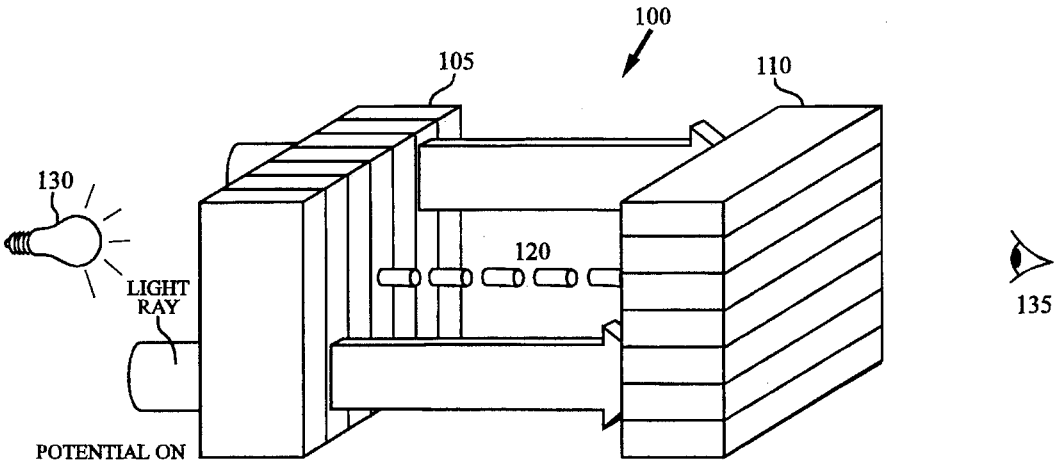


Figure 2
(Prior Art)

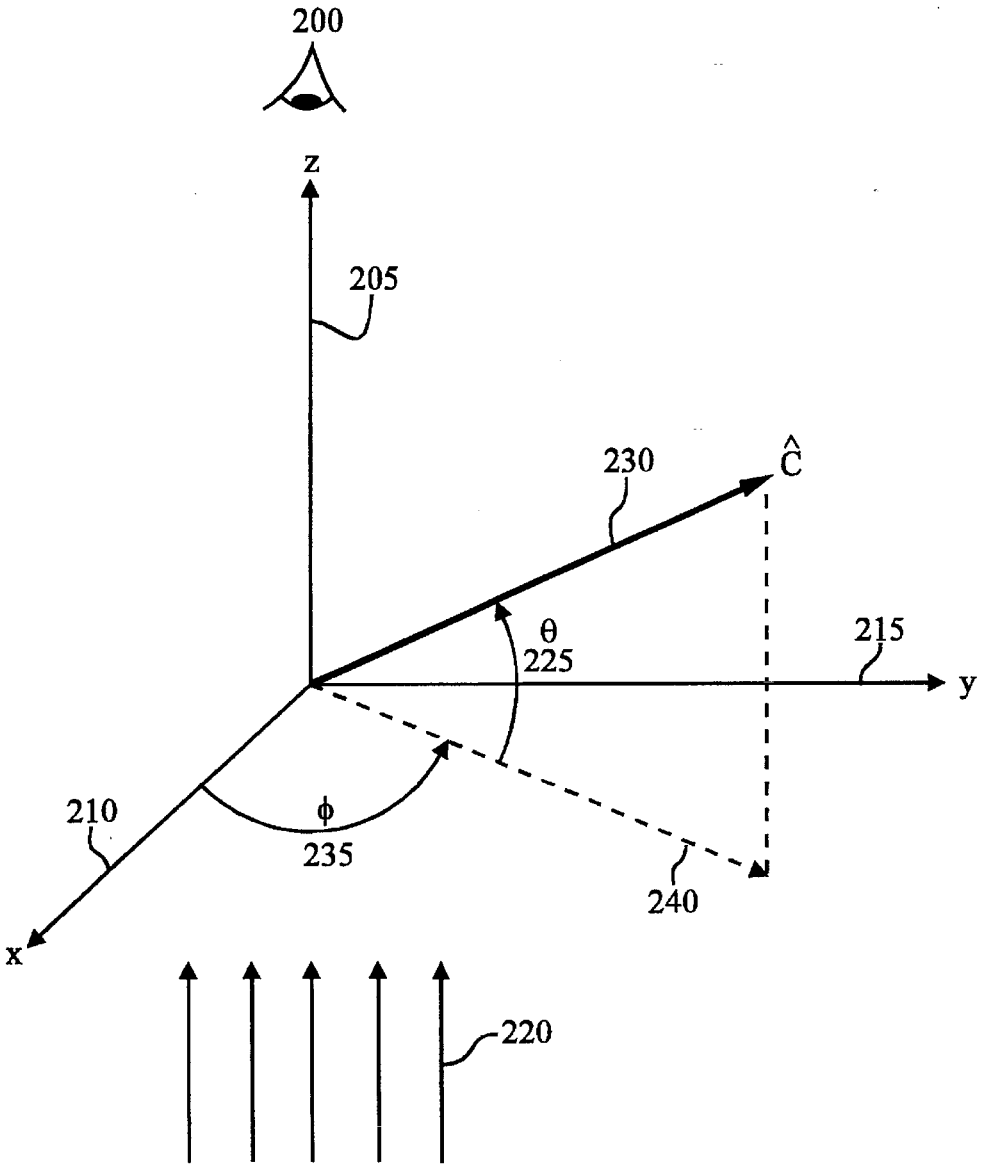


Figure 3
(Prior Art)

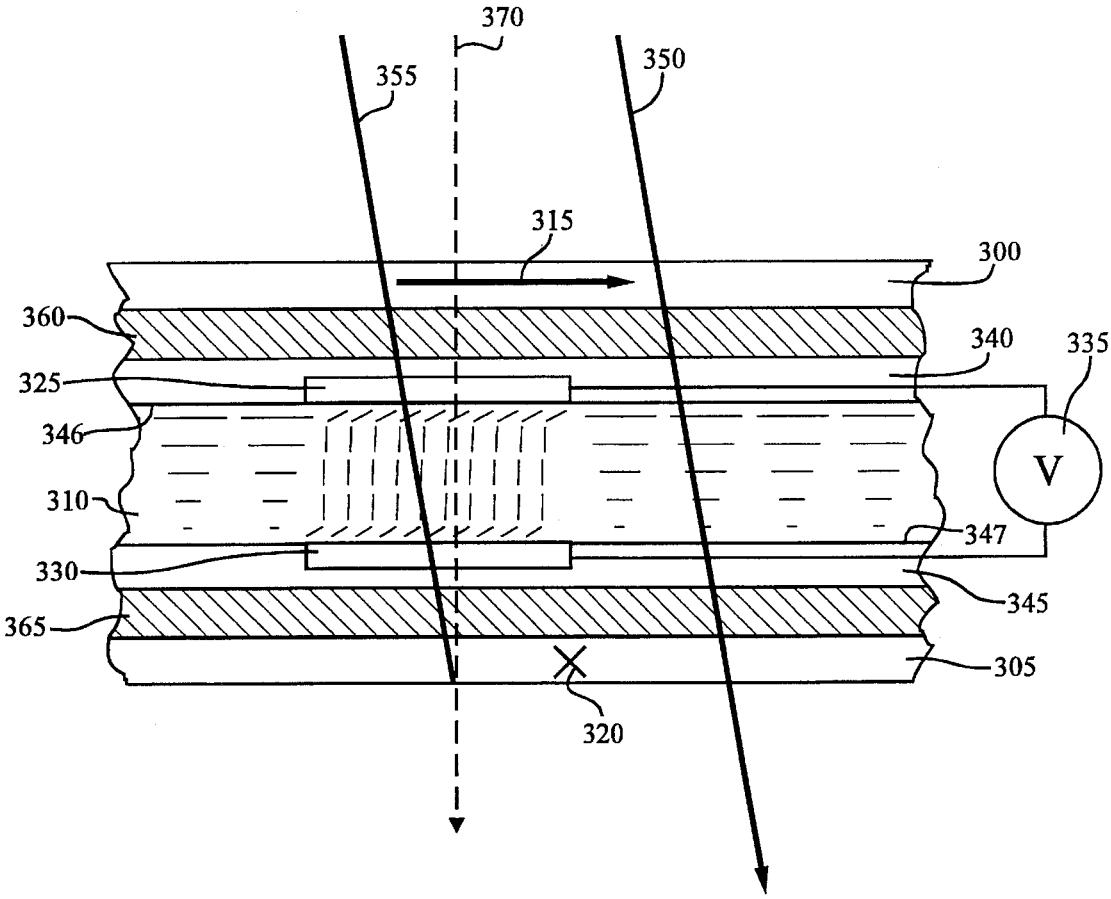


Figure 4
(Prior Art)

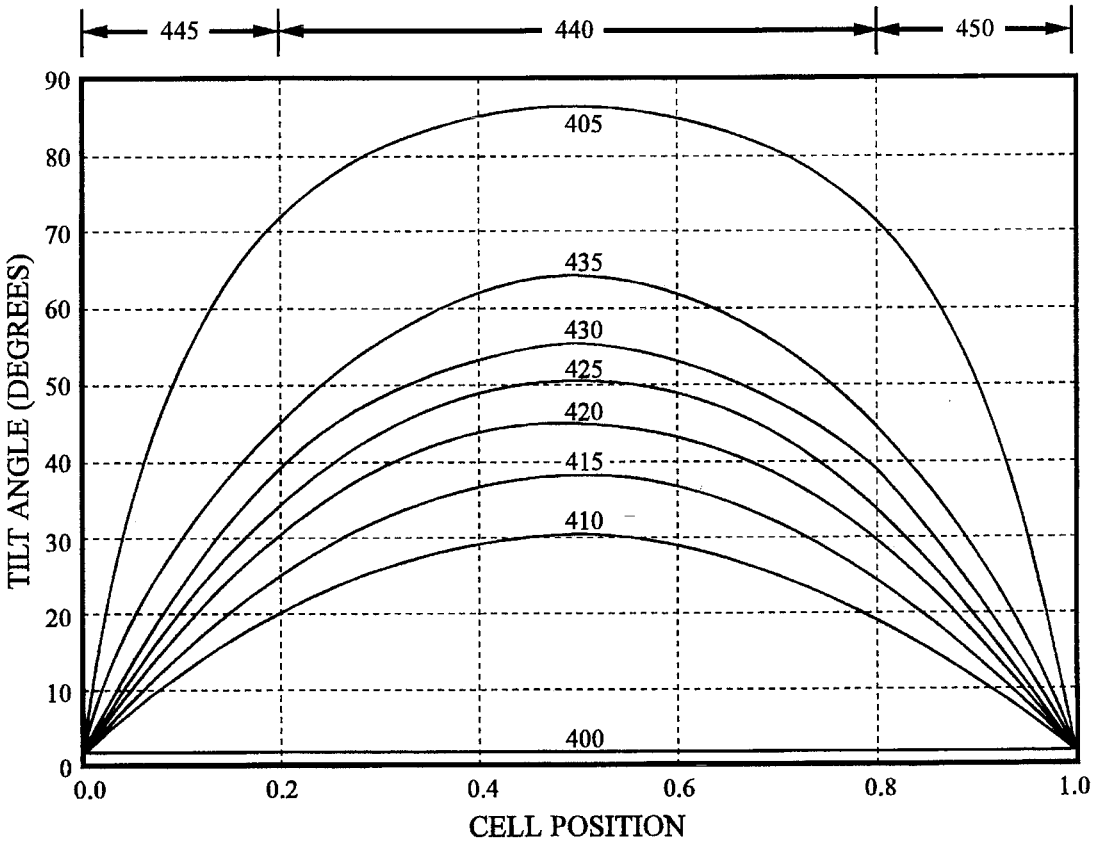


Figure 5
(Prior Art)

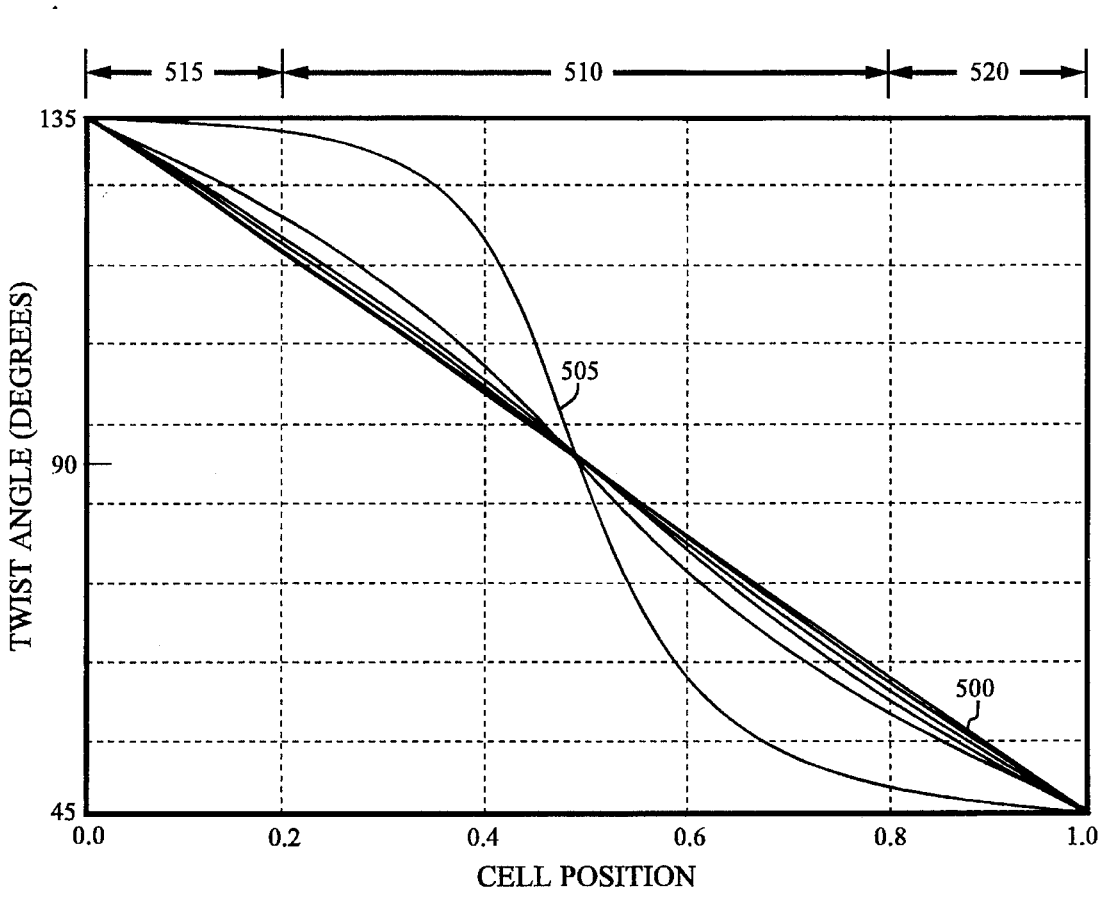


Figure 6
(Prior Art)

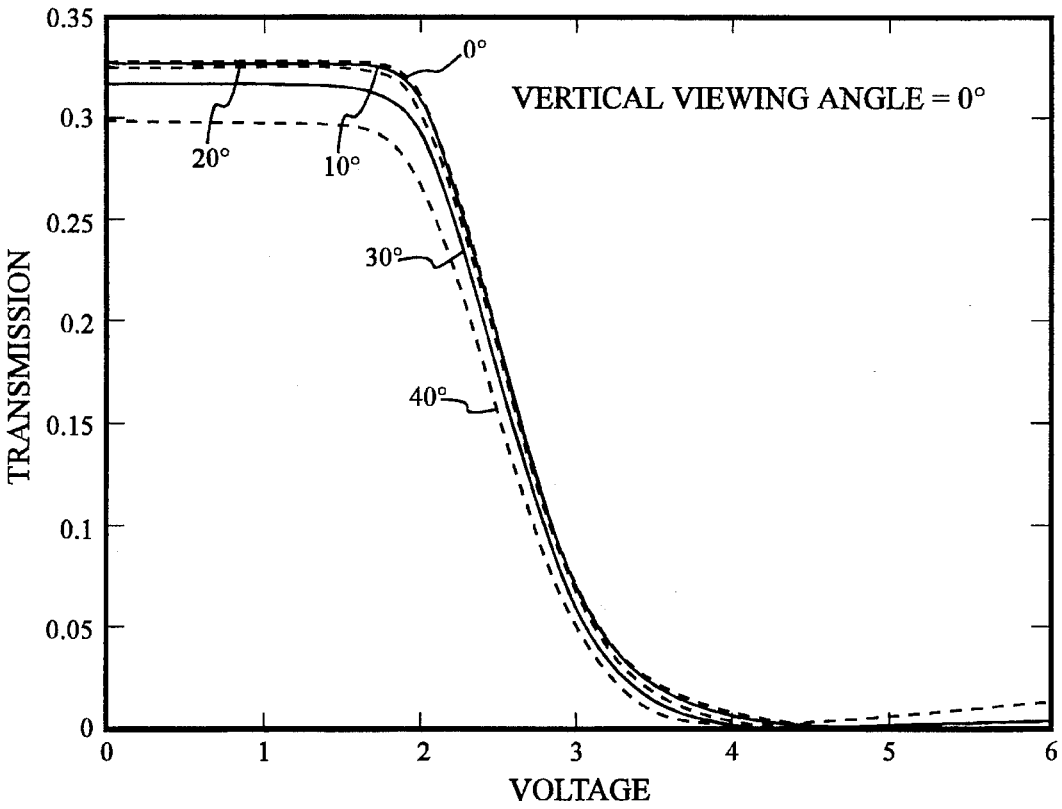


Figure 7
(Prior Art)

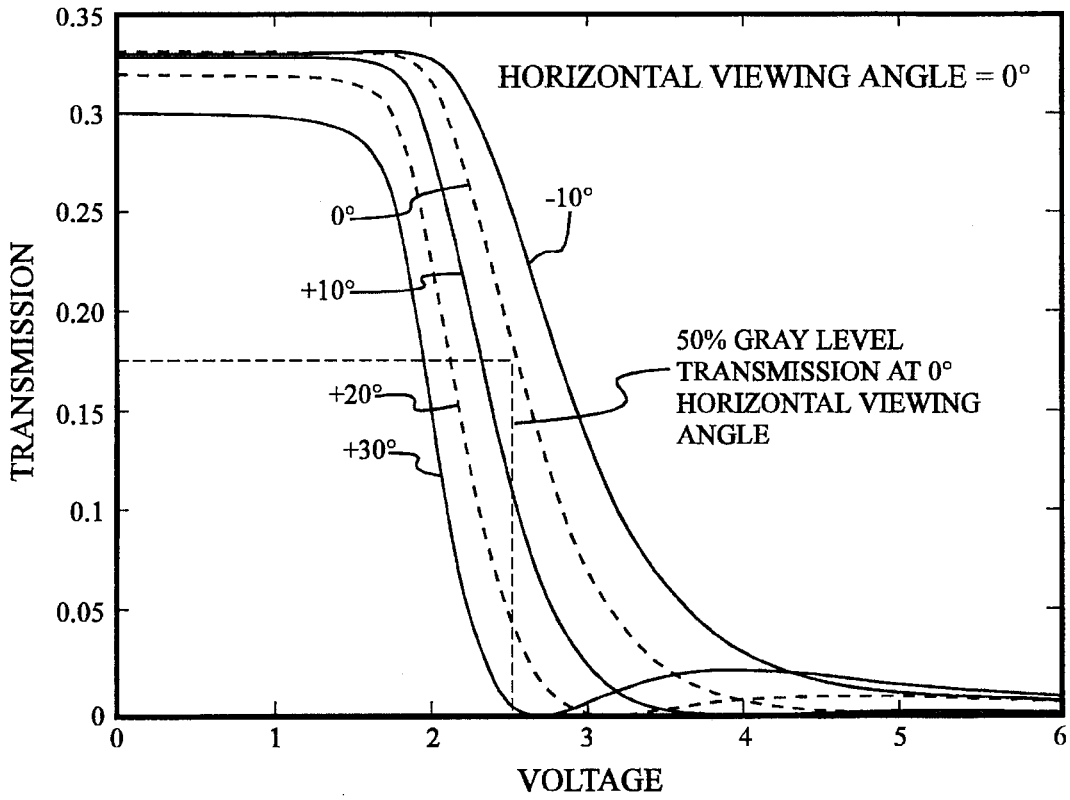


Figure 8
(Prior Art)

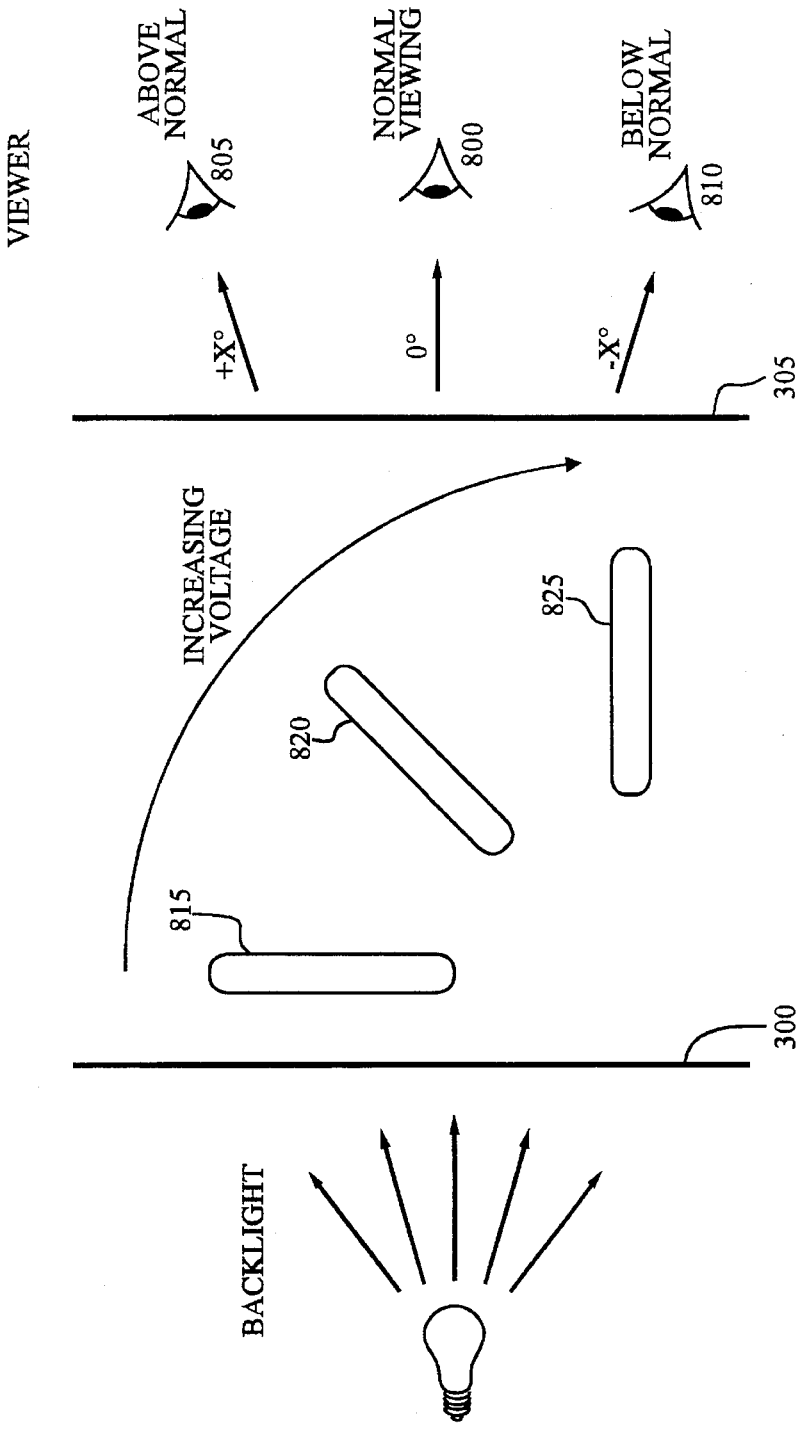


Figure 9
(Prior Art)

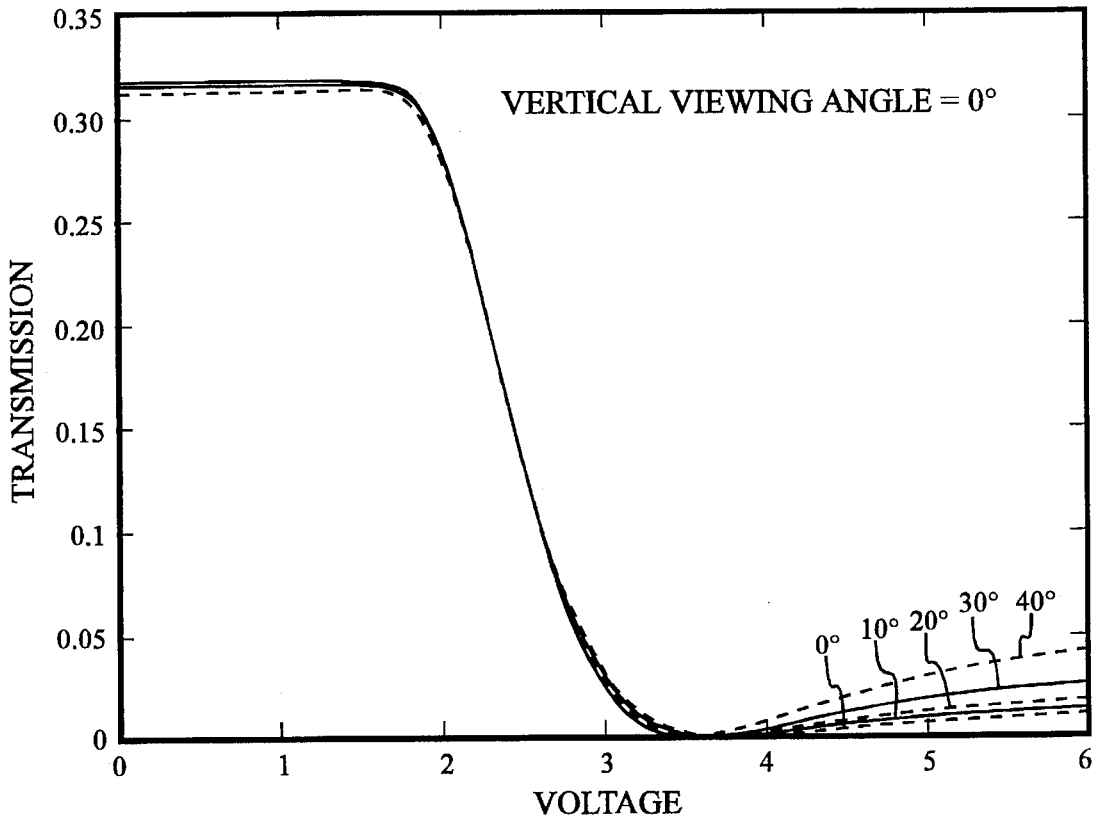


Figure 10
(Prior Art)

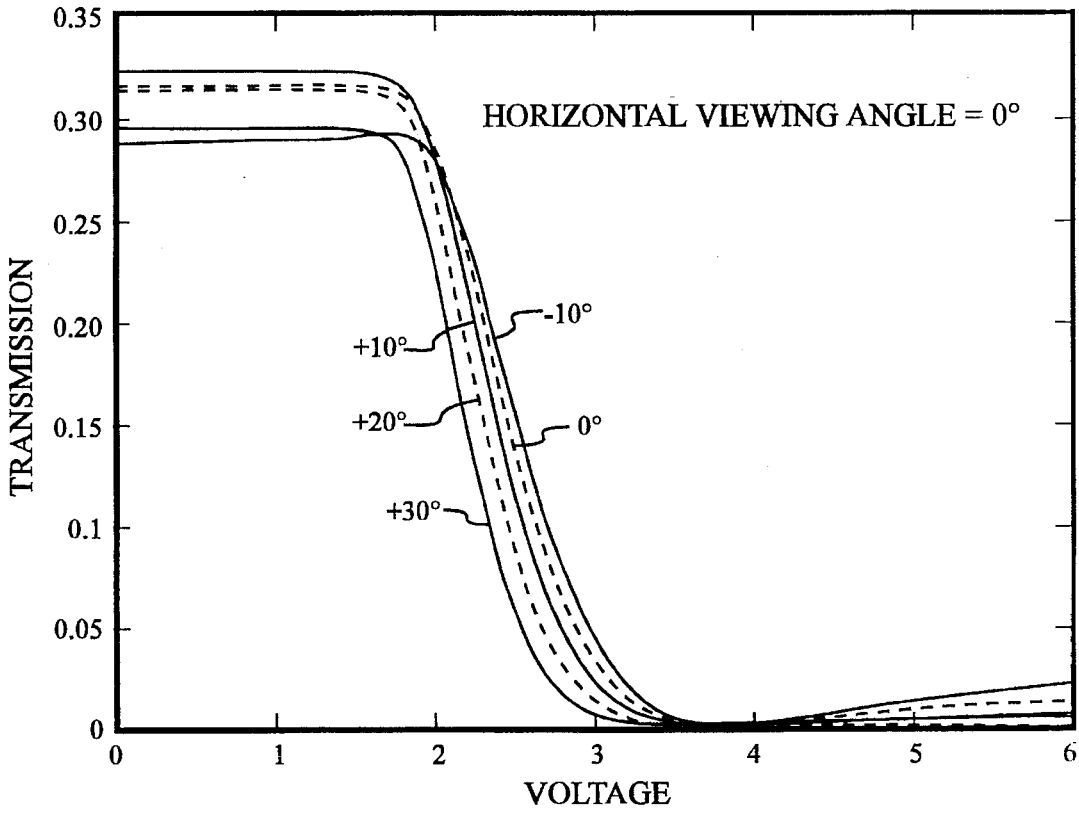


Figure 11

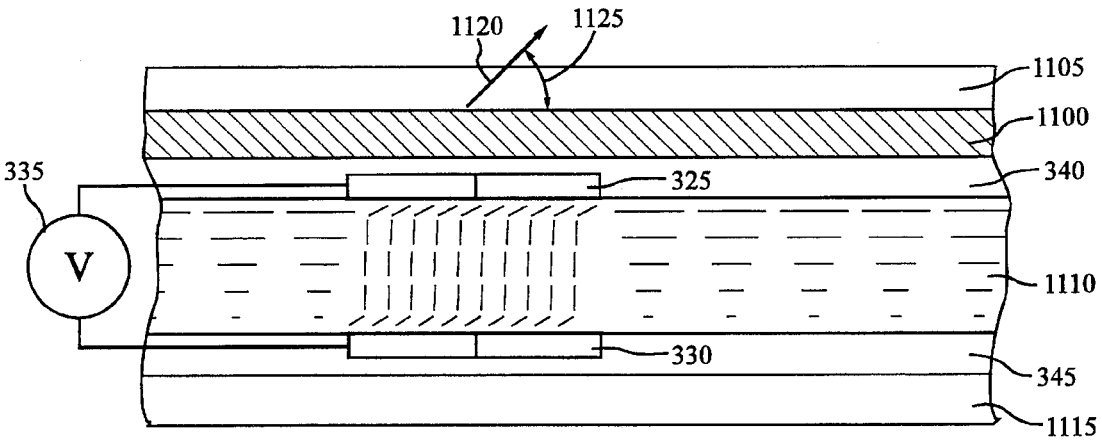


Figure 12

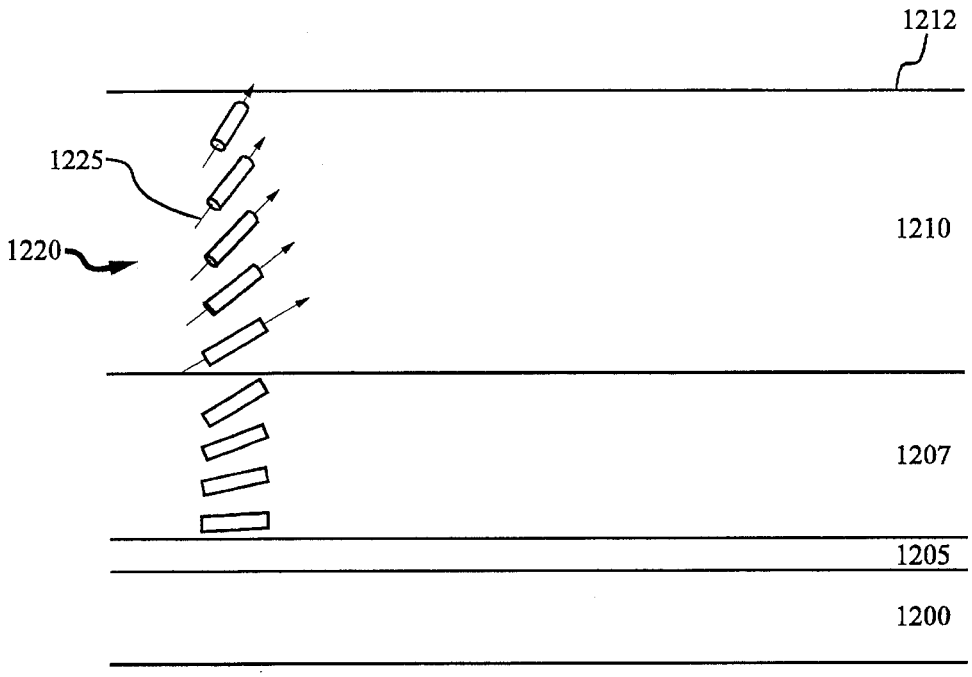


Figure 13

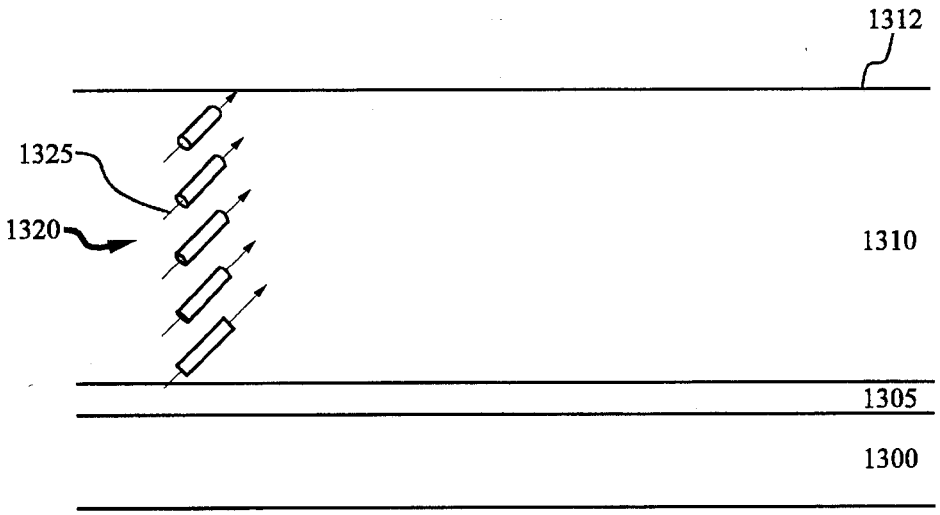
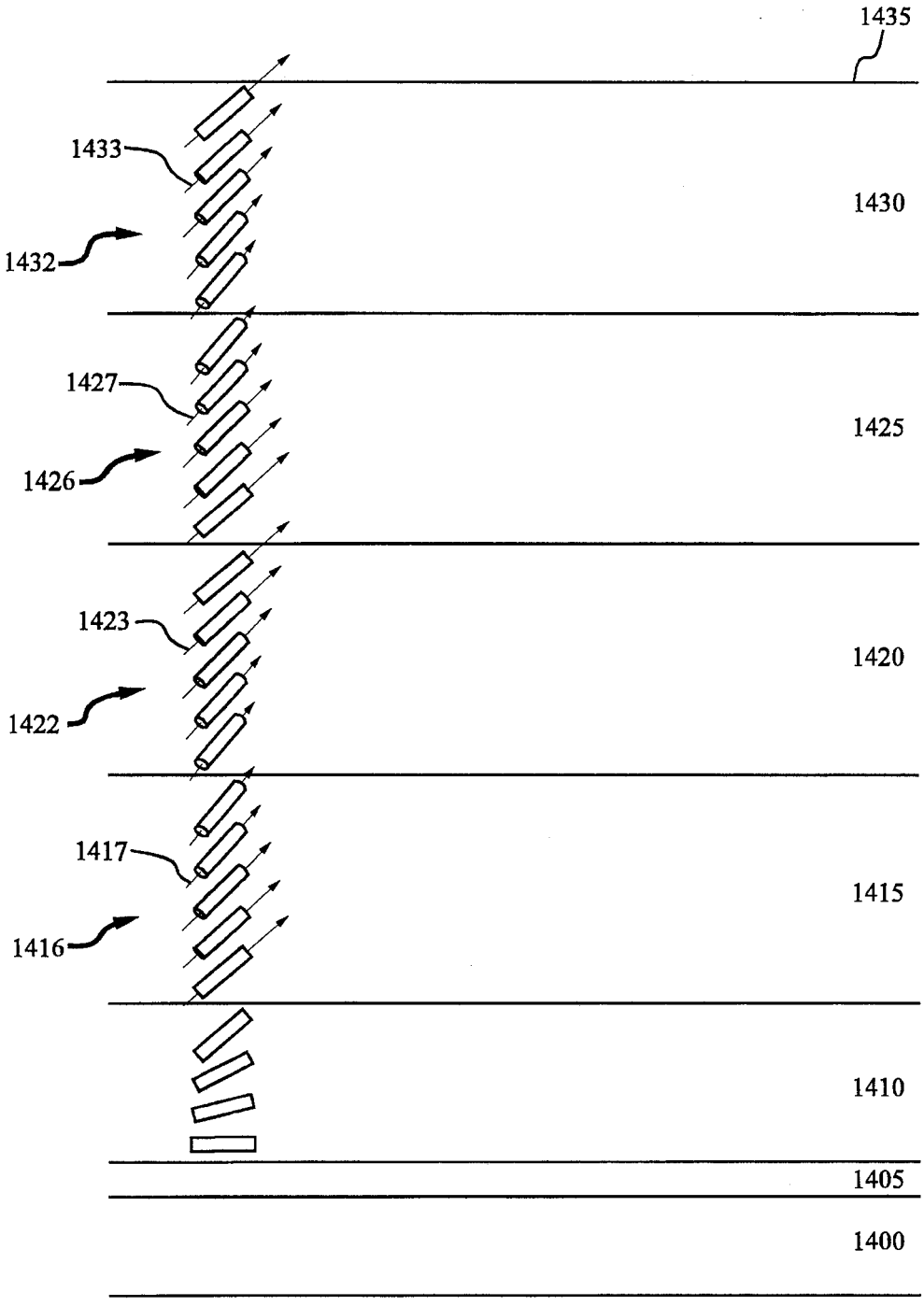


Figure 14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LCD SPLAY/TWIST COMPENSATOR HAVING VARYING TILT AND /OR AZIMUTHAL ANGLES FOR IMPROVED GRAY SCALE PERFORMANCE

REFERENCES

This application is a continuation of application Ser. No. 08/313,476 filed Sep. 30, 1994, now abandoned, which is a continuation-in-part application of U.S. patent application, Ser. No. 223,251, filed Apr. 4, 1994, now U.S. Pat. No. 5,504,603, entitled "Optical Compensator for Improved Gray Scale Performance in Liquid Crystal Display."

BACKGROUND OF THE INVENTION

This invention is concerned with the design of liquid crystal displays (LCDs) and, more particularly, with techniques for maximizing the field of view of such displays by maintaining a high contrast ratio and minimal variance in relative gray levels over a wide range of viewing angles. These goals are achieved through the fabrication and manufacture of LCDs using O-plate technology.

2.1 LCD Technology Overview

Liquid crystals are useful for electronic displays because polarized light traveling through a liquid crystal layer is affected by the layer's birefringence, which can be changed by the application of a voltage across the layer. By using this effect, the transmission or reflection of light from an external source, including ambient light, can be controlled with much less power than is required for the luminescent materials used in other types of displays. As a result, liquid crystal displays are now commonly used in a wide variety of applications, such as, for example, digital watches, calculators, portable computers, and many other types of electronic equipment. These applications highlight some of the advantages of LCD technology including very long operational life in combination with very low weight and low power consumption.

The information content in many liquid crystal displays is presented in the form of multiple rows of numerals or characters, which are generated by segmented electrodes deposited in a pattern on the display. The electrode segments are connected by individual leads to electronic driving circuitry. By applying a voltage to the appropriate combination of segments, the electronic driving circuitry controls the light transmitted through the segments.

Graphic and television displays may be achieved by employing a matrix of pixels in the display which are energized by an X-Y sequential addressing scheme between two sets of perpendicular conductors. More advanced addressing schemes, applied predominantly to twisted nematic liquid crystal displays, use arrays of thin film transistors to control driving voltages at the individual pixels.

Contrast and stability of relative gray scale intensities are important attributes in determining the quality of a liquid crystal display. The primary factor limiting the contrast achievable in a liquid crystal display is the amount of light which leaks through the display in the dark state. In addition, the contrast ratio of the liquid crystal device also depends on the viewing angle. The contrast ratio in a typical liquid crystal display is a maximum only within a narrow viewing angle centered near normal incidence and drops off as the angle of view is increased. This loss of contrast ratio is caused by light leaking through the black state pixel elements at large viewing angles. In color liquid crystal displays, such leakage also causes severe color shifts for both saturated and gray scale colors.

The viewing zone of acceptable gray scale stability in a typical prior art twisted nematic liquid crystal display is severely limited because, in addition to color shifts caused by dark state leakage, the optical anisotropy of the liquid crystal molecules results in large variations in gray level transmission, i.e., a shift in the brightness-voltage curve, as a function of viewing angle. The variation is often severe enough that, at extreme vertical angles, some of the gray levels reverse their transmission levels. These limitations are particularly important for applications requiring a very high quality display, such as in avionics, where viewing of cockpit displays from both pilot and copilot seating positions is important. Such high information content displays require that the relative gray level transmission be as invariant as possible with respect to viewing angle. It would be a significant improvement in the art to provide a liquid crystal display capable of presenting a high quality, high contrast image over a wide field of view.

FIGS. **1***a* and **1***b* show a conventional normally, white, twisted nematic liquid crystal display **100** including a polarizer **105** and an analyzer **110**. The polarizer **105** and the analyzer **110** are each bonded to glass substrates (not shown), such that the polarization axis of the analyzer **110** is perpendicular to that of the polarizer **105**. The figures also show a light source **130** and a viewer **135**.

An area between the polarizer **105** and the analyzer **110** contains a nematic liquid crystal material. The nematic phase is a fluid state of matter whose constituent molecules show long range correlation of their angular orientation (they are contained to have their long axes generally be parallel to one another), but no long range correlation of their positions in space as would be the case in a crystalline solid. The average orientation of the nematic molecules' long axes at any point in the material is called the director.

In the normally white configuration of FIGS. **1***a* and **1***b*, a "nonselect" area **115** (no applied voltage) appears light, while a "select" area **120** (those which are energized by an applied voltage) appear dark. In the nonselect area **115** the liquid crystal molecules are constrained to adopt the helical structure shown in the figure with their molecular long axes parallel to the glass substrates. In the select area **120** the liquid crystal molecules tend to tilt and rotate toward alignment with the applied electric field. The alignment state with the liquid crystal molecules' long axes normal to the surfaces of the glass substrates is termed a homeotropic alignment. In practical twisted nematic displays the applied electric fields are not strong enough to yield completely homeotropic alignment.

Many of the materials discussed in this document are birefringent. That is to say, they have varying indices of refraction depending on the direction of the electric vector of the light propagating through the material. The index of refraction is the ratio of the speed of light in a vacuum to that in the material. Materials such as liquid crystals that have different optical properties along different axes are said to be optically anisotropic. Materials without such angular variation are said to be isotropic. A uniaxial optical material has only one axis, the extraordinary axis, along which the electric vector of light interacts to yield a unique index of refraction (n_e). This index will either be the highest or lowest found in the material. In a uniaxial material all possible axes perpendicular to the extraordinary axis will yield the same index of refraction (called the ordinary index, n_O) for light

whose electric vector lies in those directions; the material has ellipsoidal symmetry. If the extraordinary axis has the highest associated refractive index value of any axis the material is said to be positively birefringent. If it has the lowest refractive index, the material is said to be negatively birefringent. Light traversing a material such that its electric vector has components along both ordinary and extraordinary axes will have one polarized component retarded in its velocity as compared to the other. If a material has a unique axis which is associated with the highest refractive index, but the axes perpendicular to it have associated refractive indices which differ one to the other, the material is said to be optically biaxial and we will refer to the axis with the associated highest index as the principal optic axis. In this document the term "optical symmetry axis" will be defined to mean the extraordinary axis in uniaxial materials and the principal optic axis in biaxial materials.

Because the liquid crystals used for twisted nematic displays exhibit positive birefringence, the homeotropic alignment state would exhibit the optical symmetry of a positively birefringent C-plate. As is well known in the art, a C-plate is a uniaxial birefringent plate with its extraordinary axis (i.e., its optic or c-axis) perpendicular to the surface of the plate (parallel to the direction of normally incident light). In the select state, the liquid crystal in a normally white display would thus appear isotropic to normally incident light, which would be blocked by the crossed polarizers.

One reason for the loss of contrast with increased viewing angle which occurs in a normally white display is that a homeotropic liquid crystal layer will not appear isotropic to off-normal light. Light propagating through the layer at off-normal angles appears in two modes due to the birefringence of the layer; a phase delay is introduced between those modes and increases with the incident angle of the light. This phase dependence on incidence angle introduces an ellipticity to the polarization state which is incompletely extinguished by the second polarizer, giving rise to light leakage. To correct for this effect, an optical compensating element must also have C-plate symmetry, but with negative birefringence ($n_e<n_o$). Such a compensator will introduce a phase delay opposite in sign to the phase delay caused by the liquid crystal layer, thereby restoring the original polarization state and allowing light passing through energized areas of the layer to be blocked more completely by the output polarizer. C-plate compensation, however, does not impact the variation of gray scale with viewing angle, which is addressed by the present invention.

FIG. **2** depicts the coordinate system which is used to describe the orientation of both liquid crystal and birefringent compensator optic axes. Light propagates toward the viewer **200** in the positive z direction **205** which, together with the x-axis **210** and the y-axis **215**, form a right-handed coordinate system. Backlighting is provided, as indicated by the arrows **220**, from the negative z direction. The polar tilt angle θ **225** is defined as the angle between the liquid crystal optic axis $\hat{C}$ **230** and the x-y plane, measured from the x-y plane. The azimuthal or twist angle Φ **235** is measured from the x-axis to the projection **240** of the optic axis onto the x-y plane.

2.2 Normally White Twisted Nematic LCDs

FIG. **3** is a cross-sectional schematic view of a prior art twisted nematic, transmissive type normally white liquid crystal display. The display includes a polarizer layer **300** and an analyzer layer **305**, between which is positioned a liquid crystal layer **310**, consisting of a liquid crystal material in the nematic phase.

It is convenient in describing the orientation of various compensation elements of the display to refer to a normal axis perpendicular to the display, which is depicted by a dashed line **370**. In the case of a normally white display, the polarizer **300** (with a polarization direction in the plane of the drawing **315**) and the analyzer **305** (with a polarization direction into the plane of the drawing **320**) are oriented with their polarization directions at 90° to one another. (A polarizer **300** and an analyzer **305** both polarize electromagnetic fields. Typically, however, the term 'polarizer' refers to a polarizer element that is closest the source of light while the term 'analyzer' refers to a polarizer element that is closest the viewer of the LCD.) The liquid crystal layer **310** is sandwiched between a pair of glass plates or substrates **340** and **345**. A first transparent electrode **325** and a second transparent electrode **330** are positioned on the glass substrates **340** and **345** adjacent to opposite surfaces of the liquid crystal layer **310** so that a voltage can be applied, by means of a voltage source **335**, across the liquid crystal layer. As is explained below, the inner surfaces **346** and **347** of the glass plates **340** and **345** and the transparent electrodes **325** and **330**, which are proximate to the liquid crystal layer **310**, can be physically or chemically treated to effect the desired liquid crystal orientation.

As is well known in the LCD art (see, e.g., Kahn, The Molecular Physics of Liquid—Crystal Devices, Physics Today, Page 68, 1982), when the inner surfaces **346** and **347** of the plates **340** and **345** are coated with a surface treatment for aligning the liquid crystal such as polyamide, buffed, and oriented with their buffed directions perpendicular, the director of the liquid crystal material, absent any applied electrical voltage, will tend to align with the buffed direction (known as the "rub direction") in the regions of the layer **310** proximate each of the plates **340** and **345**. Furthermore, the director will twist smoothly with respect to the normal axis through an angle of 90° along a path in the layer **310** from the first major surface adjacent to the plate **340** (i.e., at the **310/340** interface) to the second major surface adjacent to the plate **345** (i.e., at the **310/345** interface).

In the absence of an applied electric field, the direction of polarization of incoming polarized light will be rotated by 90° in traveling through the liquid crystal layer **310**. When the glass plates and the liquid crystal layer are placed between crossed polarizers, such as the polarizer **300** and the analyzer **305**, light polarized by the polarizer and traversing the display, as exemplified by the light ray **350**, will thus be aligned with the polarization direction of the analyzer **320** and therefore will pass through the analyzer **305**.

When a sufficient voltage is applied to the electrodes **325** and **330**, however, the applied electric field causes the director of the liquid crystal material to tend to align parallel to the field. With the liquid crystal material in this state, light passed by the polarizer **300**, as illustrated by the light ray **355**, will be extinguished by the analyzer **305**. Thus, an energized pair of electrodes will produce a dark region in the display, while light passing through regions of the display which are not subject to an applied field will produce illuminated regions. As is well known in the LCD display art, an appropriate pattern of electrodes, activated in selected combinations, can be utilized in this manner to display alphanumeric or graphic information. As explained further below, one or more compensator layers, such as the layers **360** and **365**, may be included in the display to improve the quality of the display.

2.3 Normally White Twisted Nematic LCD Characteristics

FIG. **4** shows a calculated plot of liquid crystal director tilt as a function of position in a liquid crystal layer (where the cell gap has been normalized to unity) in a 90° twisted nematic cell. Typical distributions for molecular tilt angles when no voltage is applied (curve **400**), under a typical select state voltage (curve **405**), and under the application of several intermediate voltages chosen to yield linearly spaced gray levels (curves **410**, **415**, **420**, **425**, **430**, and **435**) are shown.

FIG. **5** is a related plot for the same cell depicting the calculated twist angle (the azimuthal angle Φ of the molecular long axes given an initial rub angle azimuth of 45°) of the liquid crystal molecules as a function of position in the cell. When there is no applied voltage, the twist is distributed evenly throughout the cell (straight line curve **500**). Under a fully select state voltage, the twist angles are distributed as shown by the external, S-shaped curve **505**. The twist distributions for gray levels are shown by the intermediate curves between the two curves **500** and **505**.

As illustrated by FIGS. **4** and **5**, when the fully selected voltage is applied, nearly all of the change in twist angle experienced by the liquid crystal molecules and little of the change in tilt angle occurs in the central region of the cell. Because of this phenomena, the continuous variation of molecular orientation within the cell can be separated into three regions, each of which is characterized by its own optical symmetry. Thus, the central regions **440** (FIG. **4**) and **510** (FIG. **5**) can be considered as nominally homeotropic in the fully selected state, approximating the properties of a C-plate. The regions **445** and **450** (FIG. **4**) and **515**; and **520** (FIG. **5**), near each surface of the cell, behave as A-plates, each with its extraordinary axis aligned with the rub direction of the proximate substrate. Because there is essentially no twist in the molecules in the regions **445**, **450**, **515**, and **520**, the molecules are essentially aligned with the respective rub directions on either side of the liquid crystal layer. In addition, because the twist angle of the molecules in the regions **445**; and **515** tends to be perpendicular to the twist angle of the molecules in the regions **450** and **520**, the effect of these two regions on light traveling through the cell tends to be canceled, leaving the middle C-plate region to exert the dominant influence.

2.3(a) C-Plate Compensation

As is well known in the art, a negative C-plate compensator is designed to correct for the angle dependent phase shift introduced by propagation through the central, approximately C-plate region of a LCD cell. Such a compensator is effective to the extent that the optical symmetry of the central region dominates the selected state of the liquid crystal cell, that is, the extent to which the molecules align with the applied field. This implies that negative C-plate compensation will work best when strong fields are used for the energized state as this makes the homeotropic approximation more nearly correct. The use of a C-plate has been demonstrated to significantly reduce the leakage of the dark state over an extended field of view, thus improving contrast and reducing color desaturation.

2.3(b) Gray Scale Stability

While the C-plate compensator may be used to improve contrast it does not improve grayscale stability. The problem of maintaining constant grayscale luminance differences over the field of view relates substantially to the brightness level changes for levels assigned between the select (black for a normally white display) and nonselect (white for a normally white display) states. This phenomenon is generally depicted using transmission, or brightness versus voltage (BV) electrooptic response curves for a display to which eight gray levels are assigned, from level **0** (the select black state) to level **7** (the nonselect white state). Gray levels between **0** and **7** are chosen by assigning them a set of voltages spaced linearly in brightness along the BV curve between the select and nonselect voltages.

FIG. **6** is a plot of calculated BV curves for a normally white, 90° twisted nematic display as the horizontal viewing angle varies from 0° to 40° in 10° increments while the vertical viewing angle remains fixed at 0°. (The change in the BV curves with horizontal angle is first order independent of whether the horizontal deviation is to the left or right.) Note that the regions of each curve over which gray levels would be selected almost overlie one another for the various horizontal angles. This means that gray levels chosen to be linearly spaced at zero degrees would remain very nearly linear at even high horizontal viewing angles.

The gray scale linearity problem appears most predominantly when the vertical viewing angle varies. This is illustrated in FIG. **7**, which shows a series of BV curves for a normally white, 90° twisted nematic display as the vertical viewing angle varies from −10° to +30° while the horizontal viewing angle remains fixed at 0°. It can be observed that for angles below 0° (measured from the normal) the BV curves shift to the right (higher voltage), and fall monotonically from their maximum but fail to reach zero.

For angles above normal, the curves shift to the left and develop a rebound after an initial minimum. These effects can be explained by considering the perspectives of viewers looking at the display from above, at, and below normal, as shown in FIG. **8**. The critical feature to note is the relationship between the light traveling towards the viewer and the average liquid crystal director tilt at the center of a cell as voltage across the cell is increased.

For instance, as the voltage across a cell is increased, the average liquid crystal director in the center of the cell tilts from a parallel (with respect to the polarizer **300** and analyzer **305**) orientation **815** toward a homeotropic one **825**. For the viewer at normal incidence **800**, retardation is highest at the nonselect state voltage and lowest at the select state voltage. When the anisotropy is zero, the polarization state of the light is unchanged and it is blocked by the analyzer. Thus, the viewer sees a monotonic decrease in brightness to zero with increasing voltage.

Now consider the case of a positive vertical viewing direction (viewer above normal incidence **805**). At some intermediate voltage the average director **820** points toward the viewer and the retardation is minimal. Here the viewer sees a brightness with voltage that initially decreases toward a minimum, at the point of minimal retardation, and then increases.

For the negative vertical viewing direction (viewer below normal incidence **810**), the average director always presents a large anisotropy to a light ray, even at the highest voltage. The viewer therefore sees a monotonic decrease in brightness. Furthermore, the average liquid crystal director is always oriented at a larger angle with respect to the light ray for the below normal viewer **810** than it is for the normal incidence viewer **800**. Therefore, the anisotropy is greater and the brightness level is always higher in the negative vertical viewing direction than it is at normal incidence.

This dependency, of an LCD's brightness versus viewing angle, has a profound impact on gray scale linearity. (Note that a voltage chosen to yield a 50% gray level on the 0° curve in FIG. **7** yields a dark state on the +30° curve and approaches a fully white state at −10°.)

2.3(c) O-Plate Gray Scale Compensation

To eliminate reversal of gray levels and improve gray scale stability, a birefringent O-plate compensator can be used. The O-plate compensator principle, as described in pending U.S. patent application Ser. No. 223,251 filed on Apr. 4, 1994 utilizes a positive birefringent material with its principal optic axis oriented at a substantially oblique angle with respect to the plane of the display (hence the term "O-plate"). "Substantially oblique" implies an angle appreciably greater than 0° and less than 90°. O-plates have been utilized, for example, with angles relative to the plane of the display between 35° and 55°, typically at 45°. Moreover, O-plates with either uniaxial or biaxial materials can be used. O-plate compensators can be placed in a variety of locations between a LCD's polarizer layer and analyzer layer.

In general, O-plate compensators may also include A-plates and/or negative C-plates as well as O-plates. As is well known in the art, an A-plate is a birefringent layer with its extraordinary axis (i.e., its c-axis) oriented parallel to the surface of the layer. Its a-axis is thus oriented normal to the surface (parallel to the direction of normally incident light), leading to its designation as an A-plate. A-plates may be fabricated by the use of uniaxially stretched polymer films, such as polyvinyl alcohol, or other suitably oriented organic birefringent materials.

A C-plate is a uniaxial birefringent layer with its extraordinary axis oriented perpendicular to the surface of the layer (parallel to the direction of normally incident light). Negatively birefringent C-plates may be fabricated by the use of uniaxially compressed polymers (See, e.g., Clerc, U.S. Pat. No. 4,701,028), stretched polymer films, or by the use of physical vapor deposited inorganic thin films (See, e.g., Yeh, U.S. Pat. No. 5,196,953), for example.

Oblique deposition of a thin film by physical vapor deposition is known to produce a film having birefringent properties (see, e.g. Motohiro, Applied Optics, Volume 28, Pages 2466–2482, 1989). By further exploiting the tilted orientation of the optical symmetry axis, this process can be used to fabricate O-plates. Such components are by their nature biaxial. Their growth characteristics generate a microscopic columnar structure. The angles of the columns are tipped towards the direction of the arriving vapor stream. A deposition angle (measured from normal) of 76°, for example, results in a column angle of approximately 45°. The columns develop an elliptical cross-section as the result of shadowing. This elliptical cross-section gives rise to the biaxial character of the films. The birefringence, in magnitude and symmetry, is entirely attributable to the film microstructure and is referred to as form birefringence. These phenomena in thin films have been extensively studied and described by Macleod (Structure-related Optical Properties of Thin Films, J. Vac. Sci. Technol. A, Volume 4, No. 3, Pages 418–422, 1986).

Uniaxial O-plate components can also be used to improve grayscale stability in normally white twisted nematic LCDs. These may be fabricated by the use of suitably oriented organic birefringent materials. Those skilled in the art will recognize other means for fabricating both uniaxial and biaxial O-plates.

FIGS. **9** and **10** show the effect that an O-plate compensator can have on normally white twisted nematic display. FIG. **9** shows the BV curves for a normally white twisted nematic display using an O-plate compensator at a fixed vertical viewing angle of 0° and various horizontal viewing angles. FIG. **10** shows the BV curves for a normally white twisted nematic display using an O-plate compensator at a fixed horizontal viewing angle of 0° and various vertical viewing angles. In this example, the O-plate layer is positioned adjacent to the liquid crystal layer on the source side of the display. A-plate layers are disposed on both sides of the O-plate/liquid crystal layer stack. The variation of the BV curves versus both horizontal and vertical viewing angles is greatly reduced relative to the uncompensated case shown in FIGS. **6** and **7**.

Elimination of gray scale reversal by the use of an O-plate compensator layer occurs in the following manner. In the positive vertical viewing direction, the retardation of the O-plate increases with viewing angle and tends to offset the decreasing retardation of the liquid crystal layer. When the viewer is looking down the axis of the average liquid crystal director, the presence of the O-plate prevents the layers between the two polarizers from appearing isotropic. Thus, the rebound in the BV curve, shown in FIG. **7**, is reduced and moved to higher voltages outside of the gray scale voltage range as shown in FIG. **10**.

In the negative vertical viewing direction, the combination of an O-plate and an A-plate with their optic axes nominally at right angles tends to exhibit birefringence characteristics similar to that of a negative birefringence retarder with its optic axis oriented perpendicular to the plane containing the axes of the **0**-plate and A-plate. The direction of this retarder axis is nominally parallel to the orientation of the average liquid crystal in the central region of the cell when it is driven at a voltage between select and nonselect states. Thus, the presence of an O-plate oriented in this manner tends to cancel the birefringence of the liquid crystal layer, pulling the BV curve down, or equivalently, moving it toward the direction of lower voltages (i.e., left) as shown in FIG. **10**. A similar effect occurs in the positive and negative horizontal viewing directions as shown in FIG. **9** when compared to FIG. **6**.

The overall effect of introducing an O-plate compensator in this manner is to eliminate large rebounds in the gray scale voltage region and reduce the left-to-right shift in the BV curves as the viewing angle is varied from negative to positive vertical angles.

The orientations of the compensator optic axes can be carefully chosen so that the combined retardation effects cancel each other in the normal incidence viewing direction as well as minimize rebounds in the horizontal viewing direction. Combinations of more than one O-plate can be used as long as their orientations satisfy these requirements. Furthermore, negative C-plates can, for certain configurations, increase the contrast ratio at large fields of view, occasionally with some decrease in gray scale linearity.

2.3(d) O-Plate Technology

The liquid crystal layer, the compensator layer(s), the polarizer layer, and the analyzer layer can assume a variety of orientations relative to one another in a liquid crystal display. Some of the possible configurations which have been considered, and set out in pending U.S. patent application No. 223,251 are repeated in Table 1; where 'A' represents an A-plate, 'C' represents a C-plate, 'O' repre-

sents an O-plate, 'LC' represents the liquid crystal, and 'OxO' represents crossed O-plates. Crossed O-plates are adjacent O-plates with their azimuthal angles Φ **235** nominally crossed, one oriented between 0° and 90°; and the second oriented between 90° and 180°.

TABLE 1

Liquid Crystal Display Elements							
←Toward Rear (Polarizer Side)					Toward Front (Analyzer Side)→		
		O	A	LC			
		A	O	LC			
			O	LC	O	A	
	A	O	A	LC			
		O	A	LC	A		
	O	A	C	LC			
		OxO	A	LC			
	A	OxO	A	LC			
			A	LC	OxO	A	
A	O	A	C	LC			
		A	O	LC	O	A	
	A	O	C	LC	C	O	
	A	O	C	LC	C	O	A
	C	A	O	LC	O	A	C

The projections of the principal axes onto the plane of the display with respect to the liquid crystal director can vary with the embodiment. In some cases, for example with two O-plates, the O-plate axis projections are at 45° with respect to the average liquid crystal director, while in others, the O-plate axis is parallel with the liquid crystal director.

Crossed O-plate (OxO) designs that are further compensated with A-plates provide additional design flexibility. The choice of A-plate value is not critical as such designs can be adjusted by varying the relative orientations of the A-plates. Thus, it is possible to generate desired solutions with commercially available A-plate retardation values.

2.4 Twisted and Splayed O-plates

Computer modeling and display cell measurements show the optical behavior of the biaxial O-plate based compensators produced from Ta_2O_5 to be qualitatively different from that of compensators produced from uniaxial polymerized liquid crystal materials. For some applications, grayscale stability and contrast over field of view properties produced by the biaxial components are preferred. However, organic compensator films based on uniaxial liquid crystal polymers are very attractive because they both make a wider range of material parameters accessible and also allow the possibility of inexpensive mass production of compensator components. Therefore a goal of further compensator development has been to produce a thin film organic O-plate layer which shows biaxial character.

It is believed that biaxial compensator components produce qualitatively different optical performance because the deformation structure of the partially selected liquid crystal layer in a twisted nematic display has some biaxial character itself. In the nonselect state the liquid crystal has a helical structure which rotates the polarization state of incident light by means of the process of adiabatic waveguiding as described above. As the electric field across the liquid crystal layer is increased the helical structure is distorted and the efficiency of the waveguide decreases. Some portion of the light is no longer efficiently rotated and begins as a result to lag the rotation of the liquid crystal helical structure. This light encounters a medium intermediate in refractive index between the ordinary and extraordinary index values. The net result is that the medium appears biaxial.

The O-plate solution to the compensation of the twisted nematic display was based on the approximate model described above that the liquid crystal layer in the select state of the twisted nematic display could be divided into three regions, two A-plate-like regions and a central region of pseudo-homeotropic character. O-plate compensated displays, however, operate with the full-on black state accessible at voltages considerably reduced from the black state voltage in uncompensated displays. At these reduced drive voltages, the liquid crystal layer central region is unlikely to have completely deformed to the pseudo-homeotropic state, and the three region model becomes even more approximate. At these intermediate voltages the liquid crystal layer central region will still be significantly splayed and twisted yielding the biaxial character described in the above paragraph.

The intuitive approach to compensator development has been that like compensates like, i.e., compensators should have similar or complementary optical symmetries to the liquid crystal layers they are intended to compensate. Based on this idea and the analysis in the above paragraphs it was decided to investigate splayed and twisted O-plate structures with the idea that they could be substituted into the existing O-plate configurations described above with resulting improved performance.

2.5 Summary

When viewed at an angles nearly normal to their surfaces twisted nematic liquid crystal displays provide high quality optical characteristics, but at large viewing angles the image tends to degrade and exhibit poor contrast and grayscale stability. Compensator configurations containing O-plates have been shown to produce greatly improved contrast and grayscale stability over field of view. O-plate configurations with biaxial optical symmetry have given qualitatively different performance than those with uniaxial symmetry. It is believed that this is true because biaxial O-plates more closely approximate the symmetry of an energized twisted nematic liquid crystal layer. Currently available biaxial O-plates are produced using an expensive vacuum deposition process, and a more cost effective large volume process is desired.

It is the goal of this invention to provide a process for producing O-plates which have the desired biaxial symmetry using an inexpensive fabrication process which is capable of being scaled up to large volume production.

3. SUMMARY OF THE INVENTION

The compensator design of this invention, which includes a positively birefringent twisted and/or splayed O-plate layer, makes possible a significant improvement in the gray scale properties and contrast ratios of liquid crystal displays (LCDs) over a wide range of viewing angles. By making use of polymerized thin films of organic liquid crystal materials the compensators are able to duplicate the performance of existing biaxial inorganic O-plate compensators, but at reduced cost and with more design flexibility.

An O-plate compensator comprising an organic liquid crystal polymer thin film, and methods for fabricating the same, are disclosed. On the microscopic scale the film is composed of a polymerized birefringent liquid crystal material which is uniaxial or near uniaxial in character. The liquid crystal material is constrained such that its optical symmetry axis is, on average, oriented obliquely with the surface of the film. Within this constraint, the direction of the material's

optical symmetry axis is allowed to vary continuously along the axis normal to the film surface. If the variation is in the tilt angle of the optical symmetry axis relative to the film surface the liquid crystal material will have splayed structure. If the variation is in the azimuthal angle of the optical symmetry axis the material will have twisted structure. The invention can comprise either angular variation or both in combination.

The oblique orientation of the liquid crystal director, which is parallel to the optical symmetry axis, is achieved by casting an organic thin film onto a surface specially prepared for orienting liquid crystal monomers, such as oblique SiO, mechanically rubbed polymers, etc. The variation in tilt angle through the layer is achieved by selecting a liquid crystalline material such that its tilt angle at the substrate surface is substantially different from that at the liquid crystal air interface. The variation in azimuthal angle through the layer is achieved by doping the liquid crystal monomer with a chiral additive in sufficient quantity so as to provide the proper helical pitch along the axis normal to the film surface. The film can either be cast from a solution of the liquid crystal polymer or from a reactive liquid crystal monomer. Any solvent that may be used during the fabrication process is evaporated off and the organic thin film is annealed at a temperature in its nematic phase. If a reactive monomer is used, the film is then photopolymerized. Finally, the film is thermally quenched to 'freeze' in the liquid crystalline structure. Alternative embodiments of the splayed/twisted O-plate include the use of nematic or smectic C materials. Fabrication techniques employing these materials are described.

4. BRIEF DESCRIPTION OF DRAWINGS

FIGS. **1***a* and **1***b* show, in overview, the operation of a normally white, 90° twisted nematic liquid crystal display.

FIG. **2** depicts a coordinate system that is used to specify component orientations in the description of this invention.

FIG. **3** is a cross-sectional schematic view of a 90° twisted nematic, transmissive type normally white liquid crystal display.

FIG. **4** is a plot of the tilt angle of the director (in degrees along the vertical axis) as a function of position (as a fraction of the depth along the horizontal axis) in a 90° twisted nematic liquid crystal cell.

FIG. **5** is a related plot for the cell shown in FIG. **4**, depicting the twist angle of the liquid crystal molecules as a function of their position in the cell.

FIG. **6** is a plot of calculated brightness vs. voltage electrooptic curves at a variety of horizontal viewing directions for a typical twisted nematic display without the benefit of O-plate gray scale compensation.

FIG. **7** is a plot of calculated brightness vs. voltage electrooptic curves at a variety of vertical viewing directions for a typical twisted nematic display without the benefit of O-plate gray scale compensation.

FIG. **8** is an illustration of the viewer's perspective relative to the average director orientation of a liquid crystal display.

FIG. **9** is a plot of calculated brightness versus voltage electrooptic curves at a variety of horizontal viewing directions for a typical twisted nematic display with the benefit of O-plate gray scale compensation.

FIG. **10** is a plot of calculated brightness versus voltage electrooptic curves at a variety of vertical viewing directions for a typical twisted nematic display with the benefit of O-plate gray scale compensation.

FIG. **11** is a cross-sectional view of a normally white, twisted nematic liquid crystal display in accordance with the invention.

FIG. **12** is a cross-sectional schematic view of one embodiment of a twisted/splayed O-plate compensator stack produced by polymerization of nematic liquid crystal monomers.

FIG. **13** is a cross-sectional schematic view of one embodiment of a twisted O-plate compensator stack produced by polymerization of smectic C liquid crystal monomers.

FIG. **14** is a cross-sectional schematic view of one embodiment of a multilayer twisted/splayed O-plate compensator stack produced by polymerization of nematic liquid crystal monomers.

5. DETAILED DESCRIPTION OF A SPECIFIC EMBODIMENTS

Illustrative embodiments of the invention are described below as they might be implemented using polymeric liquid crystalline thin films to create a twisted and/or splayed O-plate compensator. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual implementation (as in any development project), numerous implementation-specific decisions must be made to achieve the developers' specific goals and subgoals, such as compliance with system- and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking of device engineering for those of ordinary skill having the benefit of this disclosure.

5.1 Introduction

FIG. **11** shows an illustrative embodiment of a liquid crystal display (LCD) system in accordance with the invention, that uses a single twisted and/or splayed O-plate compensator **1100** disposed between a polarizer **1105** and a liquid crystal layer **1110**. The O-plate layer **1100** comprises birefringent liquid crystal polymer layer having an optical symmetry axis **1120** oriented, on average, at a tilt angle **1125**, relative to the surface of the liquid crystal polymer layer **1110**, of approximately 20° to 80°. Alternatively, the O-plate layer could be located between liquid crystal layer **1110** and an analyzer **1115**, or in both locations. More details on the structure of the twisted and/or splayed O-plate layer are given below.

The decision as to where to place the O-plate compensator is purely a design choice and is, generally, based on the optical requirements of the display being compensated and on the manufacturing and cost constraints of the display system.

In general, O-plate compensators may also include A-plates and/or negative C-plates as well as O-plates. Twisted/splayed O-plate compensators may contain both twisted/splayed O-plates and simple O-plates. As is well known in the art, an A-plate is a birefringent layer with its extraordinary axis (i.e., its c-axis) oriented parallel to the surface of the layer. Its a-axis is thus oriented normal to the surface (parallel to the direction of normally incident light),

leading to its designation as an A-plate. A-plates may be fabricated by the use of uniaxially stretched polymer films, such as polyvinyl alcohol, or other suitably oriented organic birefringent materials.

5.2 Nematic Embodiment

Another illustrative embodiment, shown in FIG. **12**, includes a rigid glass substrate **1200**, an alignment layer **1205**, a polymerized pretilt nematic liquid crystal layer **1207**, an alignment/pretilt layer interface **1205/1207**, a polymerized nematic liquid crystal monomer layer **1210**, a pretilt/liquid crystal layer interface **1207/1210** and a nematic/air interface **1212**. The nematic material in the layer **1210** has been doped with a chiral dopant to yield a cholesteric pitch approximately 12 times the layer thickness, yielding a twist angle of approximately 30 degrees in the layer **1210**. The liquid crystal layers are deposited in the form of polymerizable nematic monomer compounds doped with approximately 0.5% of Igracure-651, a photoinitiator.

The alignment layer **1205** is produced by coating a surface of the substrate **1200** with a polyamide material that produces a liquid crystal pretilt angle of from 1° to 10° in the layer **1207** at the alignment/pretilt layer interface **1205/1207**. The alignment material is then rubbed so as to produce uniformly tilted alignment in the desired azimuthal orientation in the layer **1207**.

A thin film of liquid crystal monomer is applied to the alignment layer **1205** using the technique of spin coating from a solution in an inert solvent. Other methods of coating the nematic material such as, for example, dip or slot-die coating can be used as well. The solution coated onto the surface of the alignment layer **1205** may contain prepolymerized liquid crystal side-chain polymers added as a viscosity modifier to improve coating wetting characteristics. In addition, the solution should contain a photoinitiator as stated above.

After the nematic film has been applied to the alignment layer **1205**, the solvent is driven off at elevated temperature producing the pretilt layer **1207**. The temperature of the pretilt layer **1207** is adjusted so as to produce the desired nematic phase in the layer **1207** and the desired tilt angle at the **1207/1210** interface. The liquid crystal film is then illuminated with ultraviolet light (actinic radiation) at a wavelength of approximately 360 nanometers with a total exposure sufficient to polymerize the monomer to liquid crystal polymer film, thereby preserving the order of the liquid crystal phase of the layer **1207** and the desired tilt angle at the **1207/1210** interface.

The purpose of the liquid crystal pretilt layer **1207** is to provide a high pretilt alignment layer for the liquid crystal monomer used to produce the actual compensator layer **1210**. If the pretilt layer **1207** is thick enough, the pretilt angle of the material at the surface of the layer **1210** will be dictated by the nematic/air tilt angle of the material at the surface of the layer **1207**. After the application of the liquid crystal layer **1210**, the nematic/air interface of the layer **1207** becomes the pretilt/liquid crystal interface **1207/1210**. The nematic material in the layer **1207** undergoes an incremental tilting, referred to as a continuous splay/bend deformation, from the low tilt angle at the **1205/1207** interface up to the desired tilt angle at the **1207/1210** interface. For the layer **1207**, the difference between the tilt angle at the **1205/1207** interface and the tilt angle at the **1207/1210** interface is referred to as the splay angle. The pretilt layer **1207** should be sufficiently thin, approximately 100 nm., when compared to the thickness of layer the **1210**, approximately 1 μm., such that its optical retardation will be insignificant as compared to the overall retardation of the compensator stack.

Other possible alignment layer materials could be substituted for the layers **1205** and **1207** to give the required 30° pretilt angle and azimuthal alignment for the liquid crystal layer **1210**. Such materials could include, for example, mixtures of homogenous and homeotropic alignment materials that are then rubbed.

After the layer **1207** has been prepared, another layer of nematic monomer solution is deposited on its surface in a manner entirely analogous to the original deposition of the layer **1207**. After the solvent has been driven off and the material polymerized with UV irradiation, this material constitutes layer **1210**. Other methods for polymerizing thin monomer films well known in the an could be used.

The material used to prepare the layer **1210** is similar to that in **1207** with a few exceptions. The material in the layer **1210** has been doped with a chiral material as described above so as to produce an approximately 30° twist of the azimuthal orientation of the nematic optical symmetry axis (extraordinary axis). This variation in azimuthal orientation occurs about an axis normal to the layer **1210** from top to bottom through the layer **1210**. The twisted and splayed structure of the layer **1210** is represented by the liquid crystal side chains or moieties **1220**. The variation in the orientation of the optical symmetry axis of the layer **1210** is represented by the arrows **1225** projected from the moieties **1220**. As can be seen from FIG. **12**, the optical symmetry axis varies through the layer **1210** according to the tilted and azimuthal orientation of the moieties **1220** of the layer **1210**.

In this particular embodiment, the material used to produce the layer **1210** has been chosen to have a tilt angle of 60° at the nematic/air interface **1212** (the 30° pretilt angle at the **1207/1210** interface plus a 30° splay angle through the layer **1210**). The solution concentration of the nematic monomer, concentration of prepolymerized nematic polymer, and the deposition parameters are selected such that the layer **1210** is of the proper thickness to provide the required retardation value, on the order of 1 μm. A splayed/twisted O-plate layer prepared in this way will have a varying optical symmetry axis with a splay angle of 30°, a twist angle of 30°, and an average tilt angle of 45°.

5.3 Smectic C Embodiment

An alternative embodiment is shown in FIG. **13**. As before, the compensator system comprises a rigid glass substrate **1300**, an alignment layer **1305**, a polymerized liquid crystal layer **1310**, a liquid crystal/alignment layer interface **1305/1310**, and a liquid crystal/air interface **1315**. In this embodiment, however, the polymerized liquid crystal layer **1310** has a smectic C phase and a smectic C intralayer tilt angle of 45°. As such, the desired intralayer tilt angle (45°) of the liquid crystal layer **1310** remains constant through the layer **1310**.

A liquid crystal material with a smectic C to nematic phase transition rather than a smectic C to smectic A phase transition is preferred because such materials tend to have large, in the range of 10° to 45°, smectic C intralayer tilt angles.

As in the nematic embodiment, an alignment layer **1305** is produced on the surface of the substrate **1300**. In one embodiment, the alignment layer **1305** material is a thin film of silicon monoxide, SiO_x, obliquely deposited at a polar angle of approximately 60° and overcoated with a thin film

of egg lecithin, a homeotropic alignment material. This alignment layer **1305** produces a liquid crystal pretilt angle for nematic materials of approximately 80° and a uniform azimuthal direction of the liquid crystal director which is determined by the azimuthal SiO_x deposition angle.

Next, a thin film of polymerizable liquid crystal monomer is laid down on the alignment layer **1305** using techniques detailed in the nematic embodiment. The liquid crystal monomer is doped with a chiral material such that in its smectic C phase it will have a chiral pitch approximately 12 times the thickness of the layer **1310**, yielding a twist angle of approximately 30 degrees through the layer **1310**. After the solvent has been removed, the temperature of the monomer film is raised high enough to transform it into the nematic phase. The nematic phase then adopts a uniform pre-tilt angle of 80° at the liquid crystal/alignment layer interface **1305/1310**. The temperature is then slowly decreased, e.g., at a rate of approximately 0.1° C. per second, transforming the liquid crystal film into its smectic C phase.

This process forms smectic C layers parallel to the surface of the alignment layer **1305** with the molecules initially adopting a smectic C intralayer tilt angle of approximately 0°. As the temperature of the film is lowered further through its smectic C temperature range, the smectic C intralayer tilt angle increases. (The azimuthal direction of the molecules is determined by the azimuthal SiO_x deposition angle.) At a temperature just above the material's melting point, the smectic intralayer tilt angle reaches a maximum value of approximately 45°. Furthermore, in a smectic C material, the polar tilt angle at the liquid crystal/air interface **1312** does not influence the tilt angle of the bulk liquid crystal material in the layer **1310**. Various other ways to form smectic layers parallel to the alignment layer will be recognized by those skilled in the art.

As stated above, the liquid crystal monomer is doped with a chiral material to produce an approximately 30° twist of the azimuthal orientation of the liquid crystal optical symmetry axis (extraordinary axis). This variation in azimuthal orientation occurs about an axis normal to the layer **1310** from top to bottom through the layer **1310**. The azimuthal orientation of moieties **1320** at the liquid crystal/air interface **1312** is determined by a combination of the azimuthal orientation of the liquid crystal at the liquid crystal/alignment layer interface **1305/1310**, the pitch of the chiral helix in the smectic C material, and the smectic C film layer thickness. The tilted helical structure of the smectic material in the layer **1310** is represented by the moieties **1320**. The variation in the orientation of the optical symmetry axis of the layer **1310** is represented by the arrows **1325** projected from the moieties **1320**. As can be seen from FIG. **13**, the optical symmetry axis varies through the layer **1310** according to the tilted and azimuthal orientation of the moieties **1320** of the layer **1310**.

Upon obtaining the desired intralayer tilt angle in the liquid crystal film and the desired azimuthal orientation, the liquid crystal monomer film is irradiated with ultraviolet light that is sufficient to polymerize the monomer to a polymeric film **1310** in which the order of the smectic liquid crystal is preserved, typically 4–10 J/cm^2. Other polymerization techniques for thin films are well known in the an and may also be used. The result of this process is a thin film or liquid crystal layer **1310** of liquid crystal polymer that is positively birefringent and has an optical symmetry axis that is oriented at a polar tilt angle of approximately **45** ° with a twist angle of approximately 30°.

5.4 Multilayer Embodiment

A further illustrative liquid crystal display system, see FIG. **14**, includes a rigid glass substrate **1400**, an alignment layer **1405**, polymerized nematic liquid crystal pretilt layer **1410**, polymerized nematic liquid crystal layers **1415**, **1420**, **1425**, and **1430**; a liquid crystal/alignment layer interface **1405/1410**, liquid crystal/liquid crystal interfaces **1410/1415**, **1415/1420**, **1420/1425**, and **1425/1430**; and a liquid crystal/air interface **1435**.

The alignment layer **1405**, the pretilt layer **1410** and the liquid crystal layer **1415** are produced by methods identical to layers **1205**, **1210**, and **1215** in the nematic embodiment above with the following exceptions. The liquid crystal in the pretilt layer **1410** is chosen to produce a tilt angle of approximately 40° at the **1410/1415** interface after the liquid crystal layer **1415** is applied. As in the nematic embodiment above, the function of the layer **1410** is to increase the pretilt of the layer **1415** to 40° without altering the azimuthal orientation of the moieties **1416** in the layer **1415**. The liquid crystal in the layer **1415** is chosen to produce a tilt angle of 50° at the **1415/1420** interface after it is polymerized, thereby yielding a splay angle of approximately 10° through the layer **1415**.

The liquid crystal in the layer **1415** is also doped with a chiral additive so as to have a left handed cholesteric pitch of 24 times the layer thickness of the layer **1415**, yielding an approximately 15° twist of the azimuthal orientation of the nematic optical symmetry axis (extraordinary axis) through the layer **1415**. This variation in azimuthal orientation occurs about an axis normal to the layer **1415** from top to bottom through the layer **1415**. The twisted and splayed structure of the layer **1415** is represented by the liquid crystal side chains or moieties **1416**. The variation in the orientation of the optical symmetry axis of the layer **1415** is represented by the arrows **1417** projected from the moieties **1416**. As can be seen from FIG. **14**, the optical symmetry axis of the layers **1415**, **1420**, **1425** and **1430** (represented by arrows **1417**, **1423**, **1427** and **1433**) vary through the respective layers **1415**, **1420**, **1425** and **1430** according to the tilted and azimuthal orientation of the respective moieties **1416**, **1422**, **1426** and **1432** of the respective layers **1415**, **1420**, **1425** and **1430**.

After the layer **1415** has been polymerized by irradiation with UV light, the layer **1420** is applied over it. The layer **1415** functions to align layer **1420** to the proper azimuthal and pretilt (50°) orientations at the **1415/1420** interface in a manner analogous to the pretilt layer **1410** at the interface **1410/1415**. The liquid crystal in the layer **1420** is doped with a chiral additive so as to have a right handed cholesteric pitch of **24** times the thickness of the layer **1420**. As such, the layer **1420** will have a twist structure equal in magnitude (15°) yet opposite in sense to that in the layer **1415**. Additionally, the layer **1420** will have a splay angle (10°) equal in magnitude to the splay angle of the layer **1415** but opposite in sign, thereby producing a 40° tilt angle in the layer **1420** at the interface **1420/1425**.

In this particular embodiment, the layer **1415** is identical to the layer **1425**, and layer **1420** is identical to layer **1430**. The present invention, however, encompasses a multilayer embodiment in which the magnitude and sign of the tilt, splay and/or twist orientations of the successive and/or alternating layers are different in magnitude and/or in sign. Each successive layer is deposited over the preceding layer after the preceding layer has been cured with UV radiation. Each succeeding layer can be azimuthally aligned and pretilted at the interface by the preceding layer. Other

methods of polymerizing the succeeding layers may also be used. These could include thermal cure and other irradiation techniques.

The purpose of producing a layered alternating splay/twist O-plate structure as is described in this embodiment is to yield a compensator which has a biaxial nature, but which has minimum twisting power for polarized light which transits the compensator stack.

5.5 Possible Variations

For each of the previous illustrative embodiments, a number of variations are possible and would be obvious to one skilled in the art of liquid crystal display devices. For example, other possible substrate materials could include non-birefringent polymer films. The polymerizable liquid crystal monomer material may include, as a constituent, molecules that contain two reactive functional groups and therefore can act as cross-linking agents. Other polar tilt angles at the liquid crystal/alignment layer interface can be achieved by suitable selection of reactive liquid crystals, modification of the alignment materials, rubbing conditions, etc. Furthermore, a non-reactive liquid crystal material can be combined with the polymerizable liquid crystal. The resulting liquid crystal polymer film would then have the properties of a plastic or gel. The liquid crystal material could also contain a polymer, liquid crystal polymer, or oligomer that increases the viscosity of the liquid crystal mixture and improves the film forming properties thereof.

Additionally, the various embodiments have been described above with specific pretilt, splay and twist orientations and/or angles, but the present invention is not limited to specific angles or orientations. Finally, the multilayer embodiment has been specifically described with nematic layers but the multilayer embodiment can be of multiple smectic C layers.

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It will be appreciated by those of ordinary skill having the benefit of this disclosure that numerous variations from the foregoing illustration will be possible without departing from the inventive concept described herein. Accordingly, it is the claims set forth below, and not merely the foregoing illustrative embodiments, which are intended to define the exclusive rights claimed in this application program.

What is claimed is:

1. A compensator for a liquid crystal display, wherein:

(a) said compensator comprises a layer of a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and a azimuthal angle, measured relative to the plane of the layer;

(b) said birefringent material comprises a polymer matrix including polymerized nematic material and unpolymerized nematic material;

(c) each of said tilt angle and said azimuthal angle varies along an axis normal to said layer, said tilt angle limited to values between approximately 25 degrees and approximately 65 degrees; and

(d) said variations in tilt angle and azimuthal angle being defined by a combination of molecular orientations of said polymerized nematic material and said unpolymerized nematic material.

2. A compensator for a liquid crystal display, said compensator comprising a layer of a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein said azimuthal angle varies along an axis normal to said layer, and said tilt angle is substantially fixed at an angle between approximately 25 degrees and approximately 65 degrees, along an axis normal to said layer.

3. A compensator for a liquid crystal display, said compensator comprising a layer of a birefringent material having an optical summetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein said tilt angle varies along an axis normal to said layer, and said azimuthal angle is substantially fixed along an axis normal to said layer.

4. A compensator for a liquid crystal display, said compensator comprising a layer of a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein each of said tilt angle and said azimuthal angle varies along an axis normal to said layer.

5. The compensator of claim **2**, wherein said layer of birefringent material comprises a polymer matrix that defines said variation of the optical symmetry axis, said polymer matrix comprising polymerized nematic material.

6. The compensator of claim **2**, wherein said layer of birefringent material comprises a polymer matrix, said polymer matrix including polymerized nematic material and unpolymefized nematic material having respective molecular orientations which, in combination, define said variation of the optical symmetry axis.

7. The compensator of claim **2** further comprising one or more A-plate layers.

8. The compensator of claim **2**, further comprising one or more C-plate layers.

9. The compensator of claim **3**, wherein said layer of birefringent material comprises a polymer matrix that defines said variation of the optical symmetry axis, said polymer matrix comprising polymerized nematic material.

10. The compensator of claim **3**, wherein said layer of birefringent material comprises a polymer matrix, said polymer matrix including polymerized nematic material and unpolymerized nematic material having respective molecular orientations which, in combination, define said variation of the optical symmetry axis.

11. The compensator of claim **3** further comprising one or more A-plate layers.

12. The compensator of claim **3** further comprising one or more C-plate layers.

13. The compensator of claim **4**, wherein said layer of birefringent material comprises a polymer matrix that defines said variation of the optical symmetry axis, said polymer matrix comprising polymerized nematic material.

14. The compensator of claim **4**, wherein said layer of birefringent material comprises a polymer matrix, said polymer matrix including polymerized nematic material and

unpolymerized nematic material having respective molecular orientations which, in combination, define said variation of the optical symmetry axis.

15. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, each layer in accordance with claim **4**, wherein the tilt angles of adjacent said layers vary in a positive sense and a negative sense respectively.

16. The compensator of claim **4** further comprising one or more A-plate layers.

17. The compensator of claim **4** further comprising one or more C-plate layers.

18. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, each layer in accordance with a specified one of claims **2**, **3**, and **4**.

19. The compensator of claim **18**, wherein (1) the birefringent material in each said layer includes a plurality of moieties of a liquid crystal material, and (2) a specified said layer aligns the moieties of liquid crystal material in an adjacent said layer.

20. The compensator of claim **19** further comprising one or more C-plate layers.

21. The compensator of claim **19** further comprising one or more A-plate layers.

22. The compensator of claim **18** further comprising one or more A-plate layers.

23. The compensator of claim **18** further comprising one or more C-plate layers.

24. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, each layer comprising a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein said azimuthal angle varies along an axis normal to said layer, and said tilt angle is substantially fixed at an angle between approximately 25 degrees and approximately 65 degrees, along an axis normal to said layer, wherein the optical symmetry axes of adjacent said layers vary azimuthally in a positive sense and a negative sense respectively.

25. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, each layer comprising a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein said tilt angle varies along an axis normal to said layer, and said azimuthal angle is substantially fixed along an axis normal to said layer and wherein the tilt angles of adjacent said layers vary in a positive sense and a negative sense respectively.

26. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, wherein:

(a) each layer comprises a birefringent material including a plurality of moieties of a liquid crystal material;

(b) the optical symmetry axis of each layer has a respective tilt angle, relative to the plane of the layer, which varies along an axis normal to the layer, with the tilt angles of adjacent said layers varying in a positive sense and a negative sense respectively;

(c) the optical symmetry axis of each layer has a respective azimuthal angle, relative to a reference axis in the plane of the layer, which varies along an axis normal to said layer, with the azimuthal angles of adjacent said layers varying in a positive sense and a negative sense respectively; and

(d) a specified said layer aligns the moieties of liquid crystal material in an adjacent said layer.

27. A compensator for a liquid crystal display, said compensator comprising a plurality of layers, each layer comprising a birefringent material having an optical symmetry axis defined by a tilt angle, measured relative to the plane of the layer, and an azimuthal angle, measured relative to a reference axis in the plane of the layer, wherein each of said tilt angle and said azimuthal angle varies along an axis normal to said layer, and wherein the optical symmetry axes of adjacent said layers vary azimuthally in a positive sense and a negative sense respectively.

28. A liquid crystal display for viewing at various angles with respect to a normal axis perpendicular to the display, comprising:

(a) (a) a polarizer layer;

(b) (b) an analyzer layer;

(c) (c) a liquid crystal layer disposed between the polarizer layer and the analyzer layer;

(d) (d) a first electrode proximate to a first major surface of the liquid crystal layer;

(e) (e) a second electrode-proximate to a second major surface of the liquid crystal layer, the first and second electrodes being adapted to apply a voltage across the liquid crystal layer when the electrodes are connected to a source of electrical potential; and

(f) (f) a compensator in accordance with a specified one of claim **1**, **5**, **6**, **2**, **3**, **4**, **24**, **28**, **26**, **7**, **8**, **9**, **13**, **10**, **14**, **27**, **15**, **11**, **16**, **12** and **17** disposed between the polarizer layer and the analyzer layer.

29. The liquid crystal display of claim **28**, wherein said compensator is optically matched with said liquid crystal layer to provide a desired viewing characteristic over a specified field of view.

* * * * *

EXHIBIT G

US006734926B2

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Fan et al.

(10) **Patent No.: US 6,734,926 B2**
(45) **Date of Patent: May 11, 2004**

(54) **DISPLAY APPARATUS WITH A REDUCED THICKNESS**

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(73) Assignee: **Chi Mei Optoelectronics Corporation**, Tainan (TW)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/065,039**

(22) Filed: **Sep. 13, 2002**

(65) **Prior Publication Data**

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(52) **U.S. Cl.** **349/58**; 349/58; 349/149; 349/150; 349/151; 349/152
(58) **Field of Search** 349/58, 149–152

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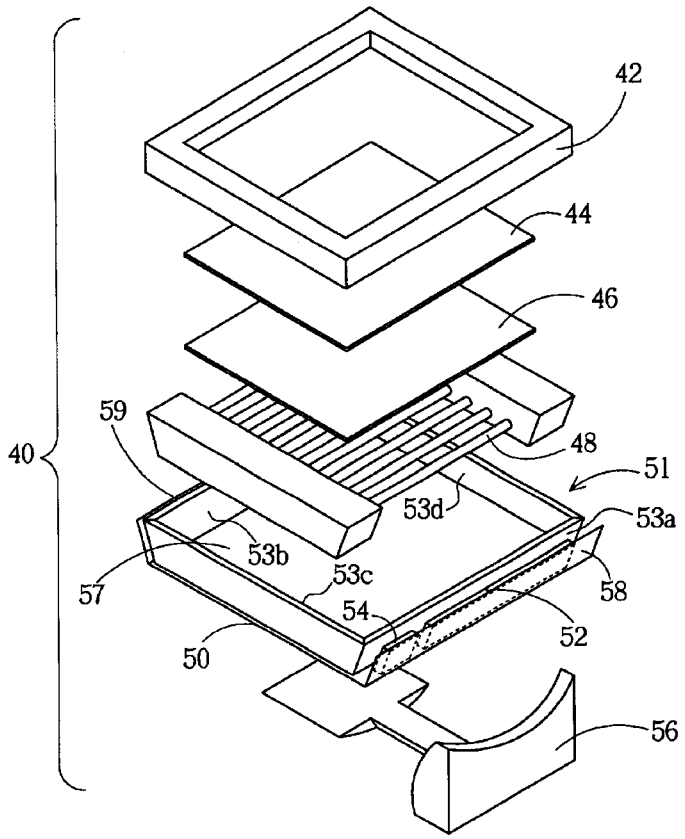
Primary Examiner—Michael G. Lee
Assistant Examiner—Seung H Lee
(74) *Attorney, Agent, or Firm*—Winston Hsu

(57) **ABSTRACT**

An LCD apparatus with a reduced thickness comprises an upper frame to protect internal components, a display panel installed inside the upper frame, a light tube array disposed behind the display panel, a reflecting plate behind the light tube array, a supporting frame installed on the reflecting plate for supporting the display panel, and a circuit board for controlling the operation of the LCD apparatus. The reflecting plate comprises a main portion and a plurality of side portions. The circuit board is an integration of all control boards using printed circuit board assembly technology and is disposed on at least one of the side portions of the reflecting plate. The main portion of the reflecting plate serves as another frame and is coupled to an end of a stand assembly to support the LCD apparatus.

42 Claims, 13 Drawing Sheets



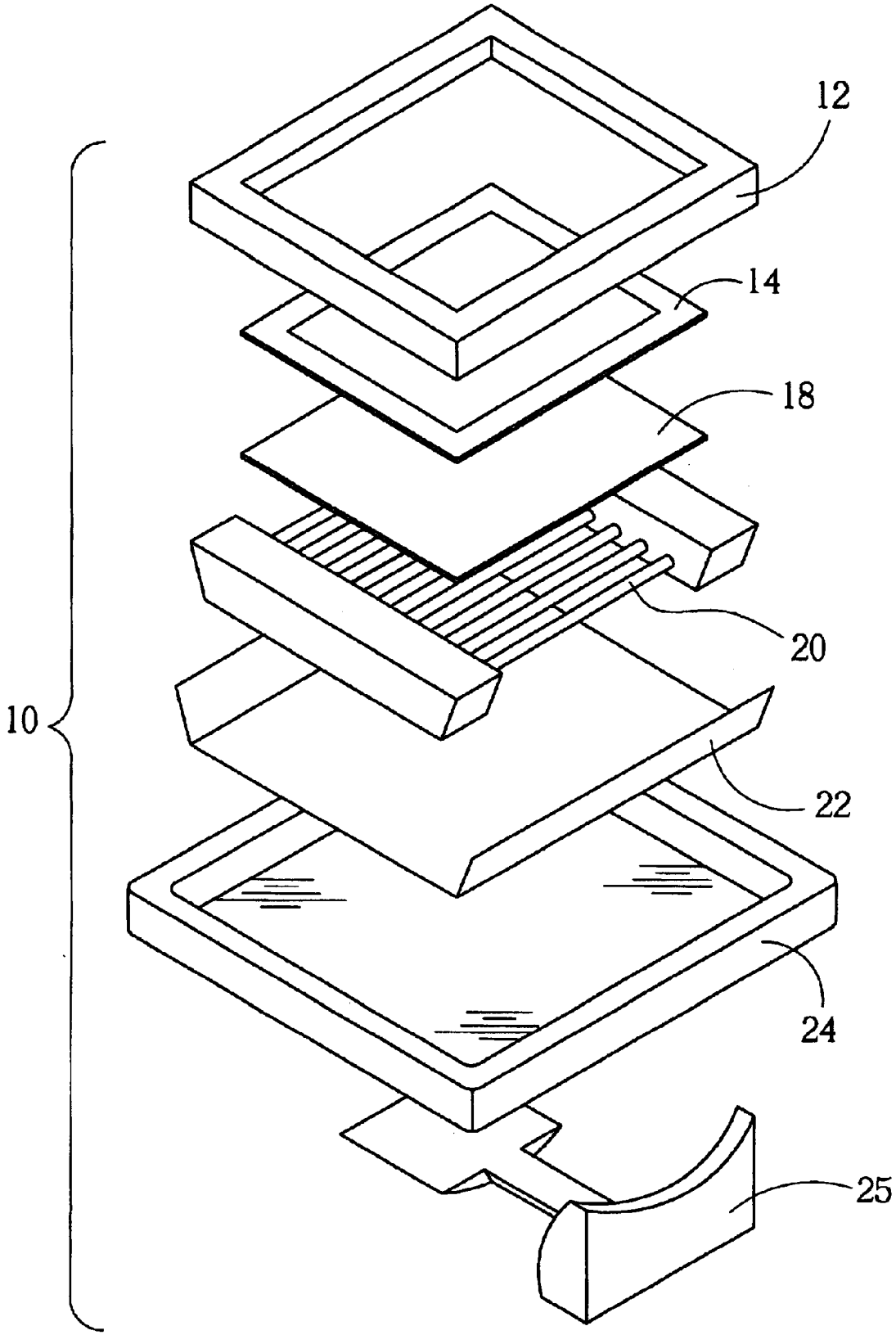


Fig. 1 Prior art

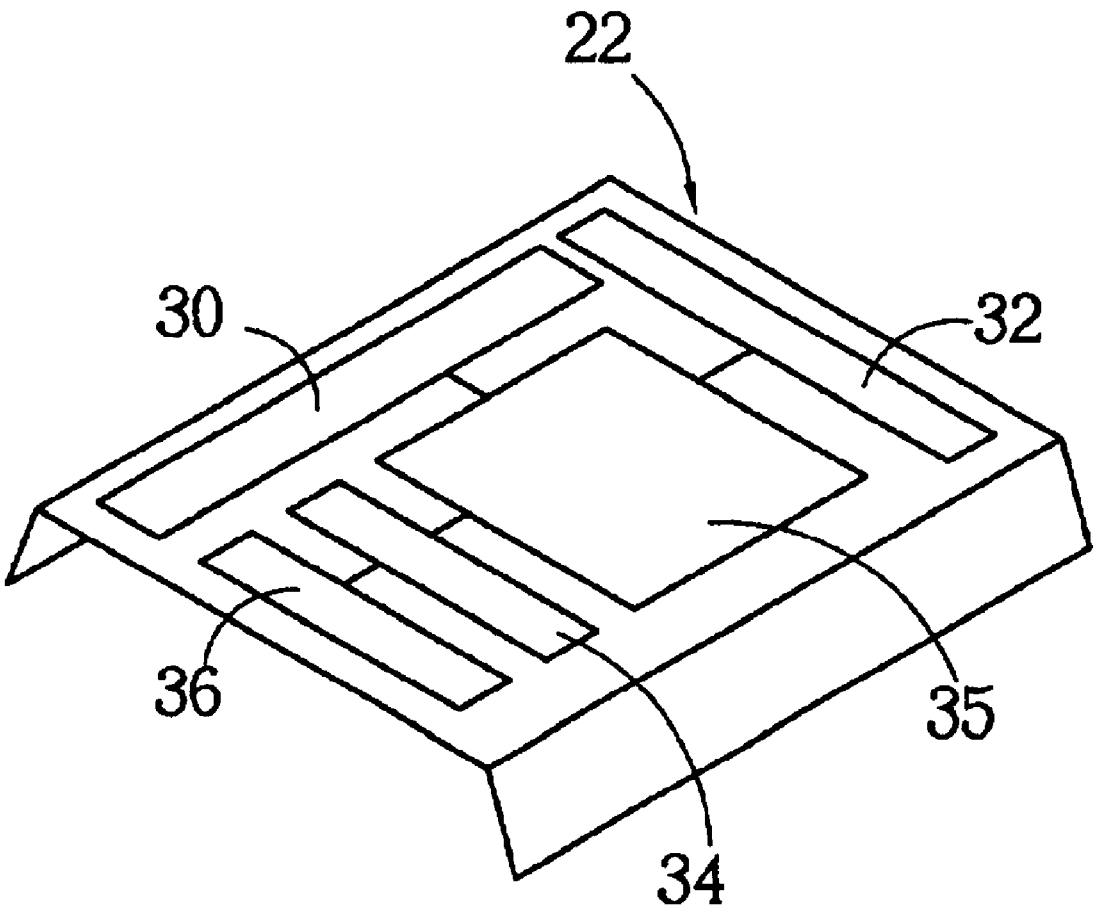


Fig. 2 Prior art

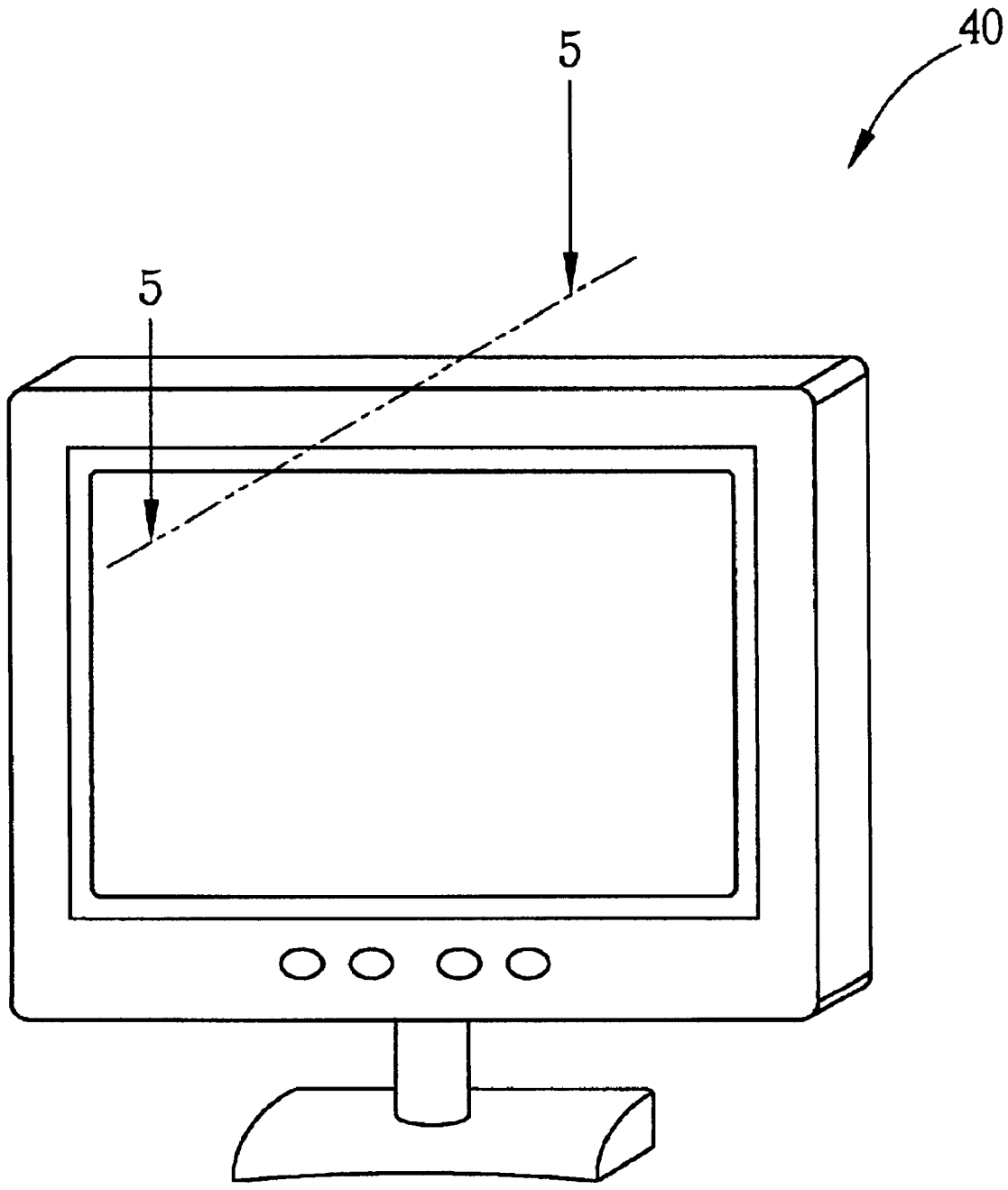


Fig. 3

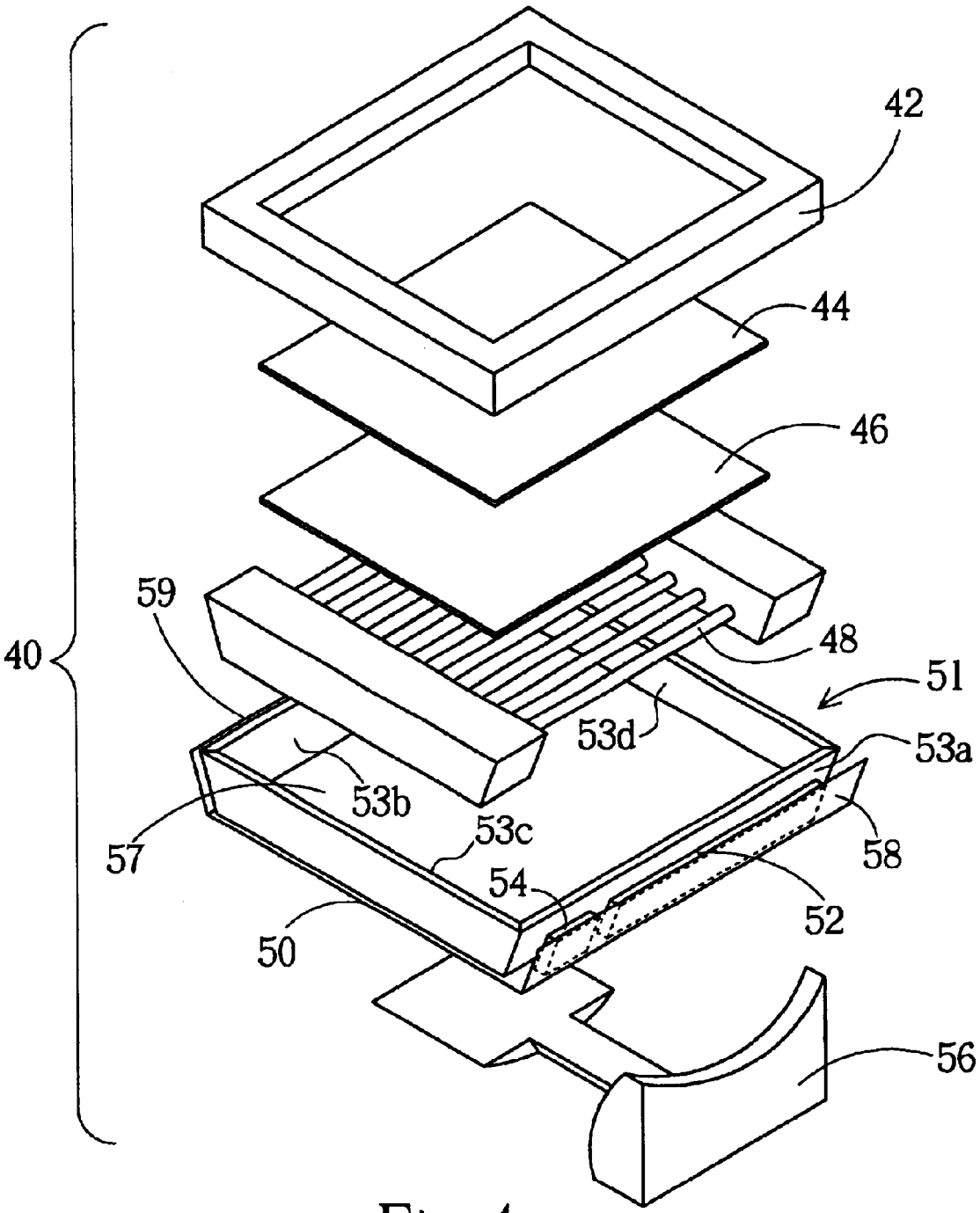


Fig. 4

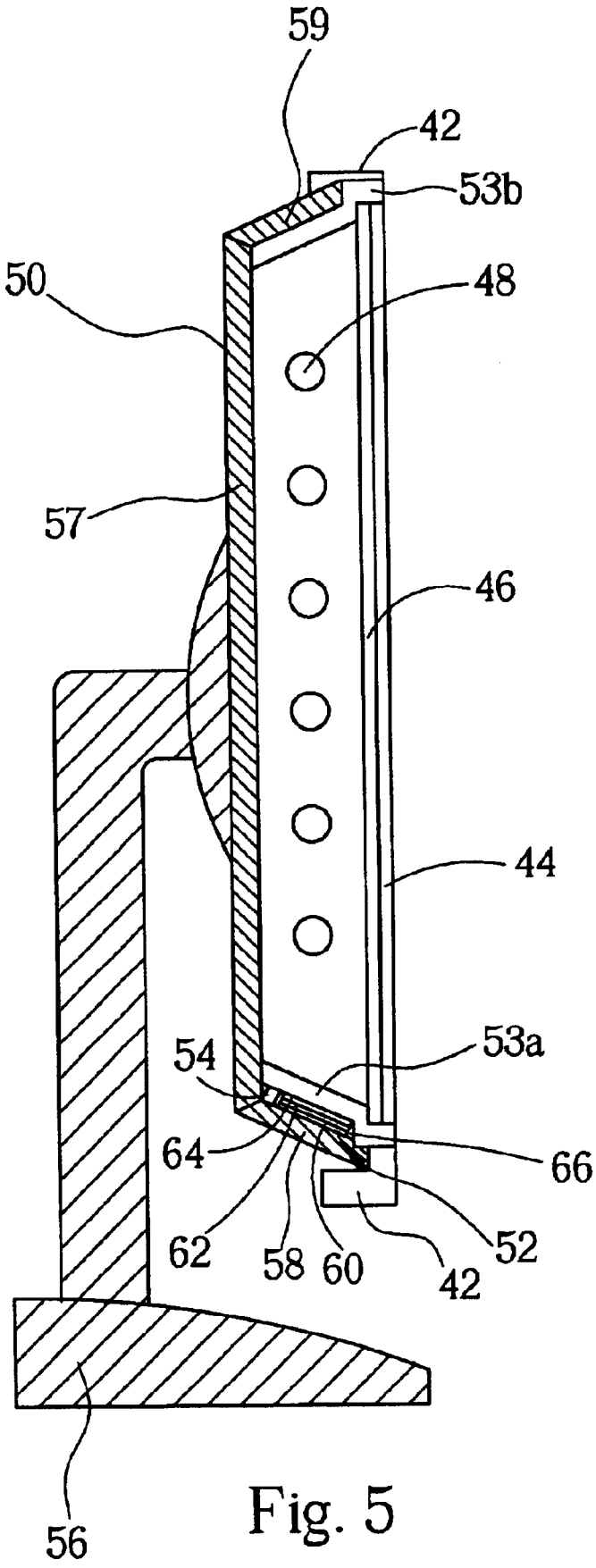


Fig. 5

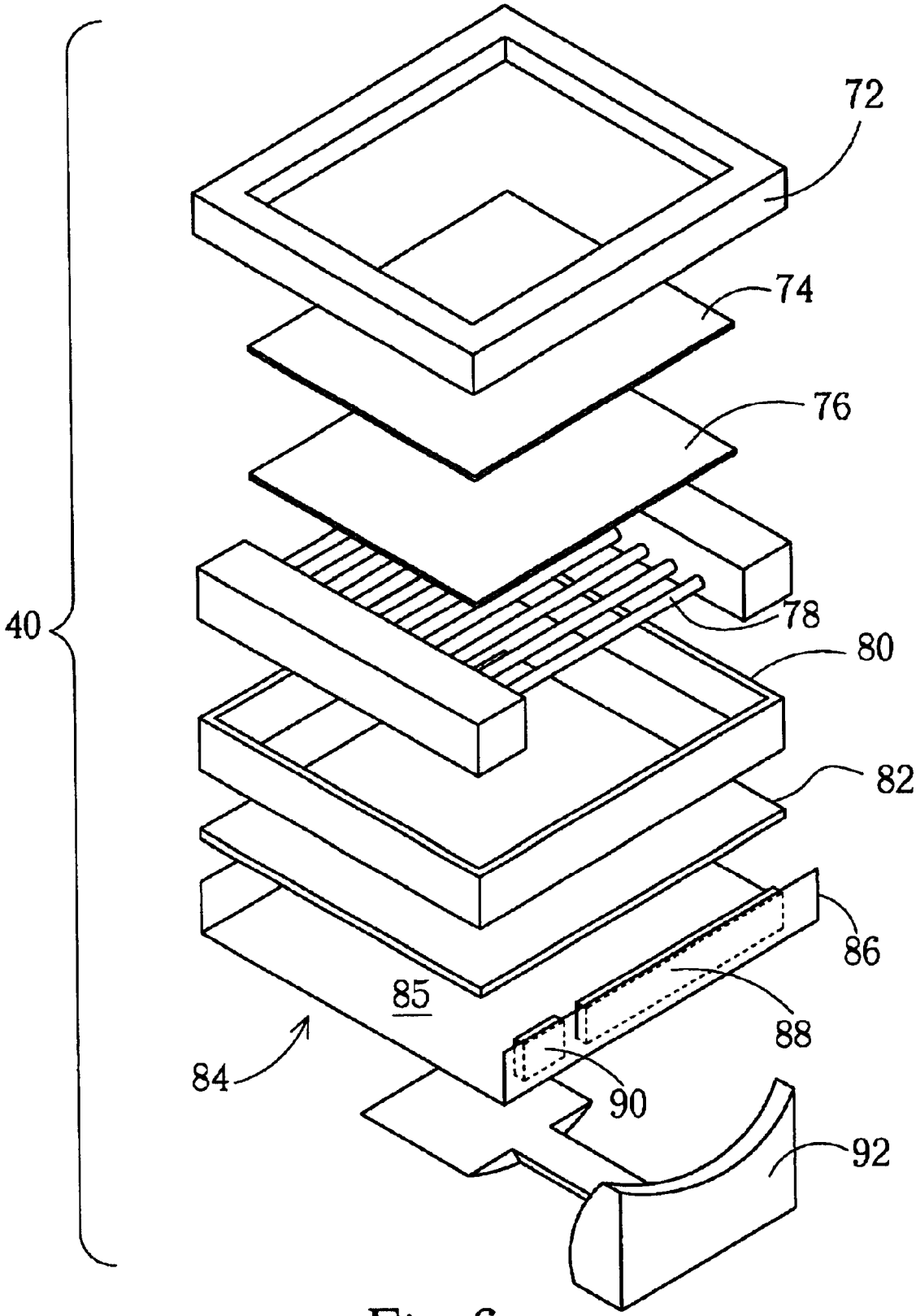


Fig. 6

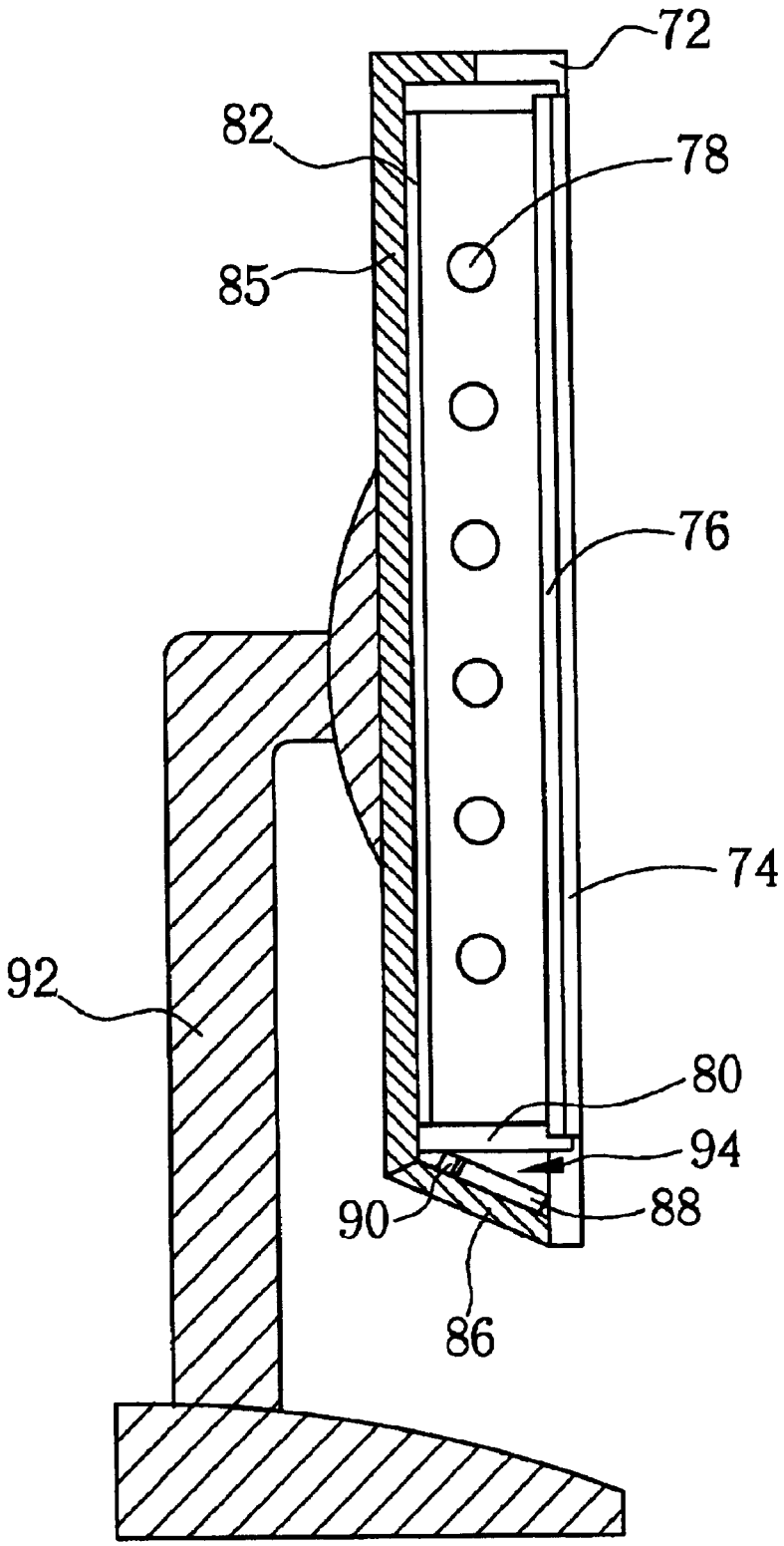


Fig. 7

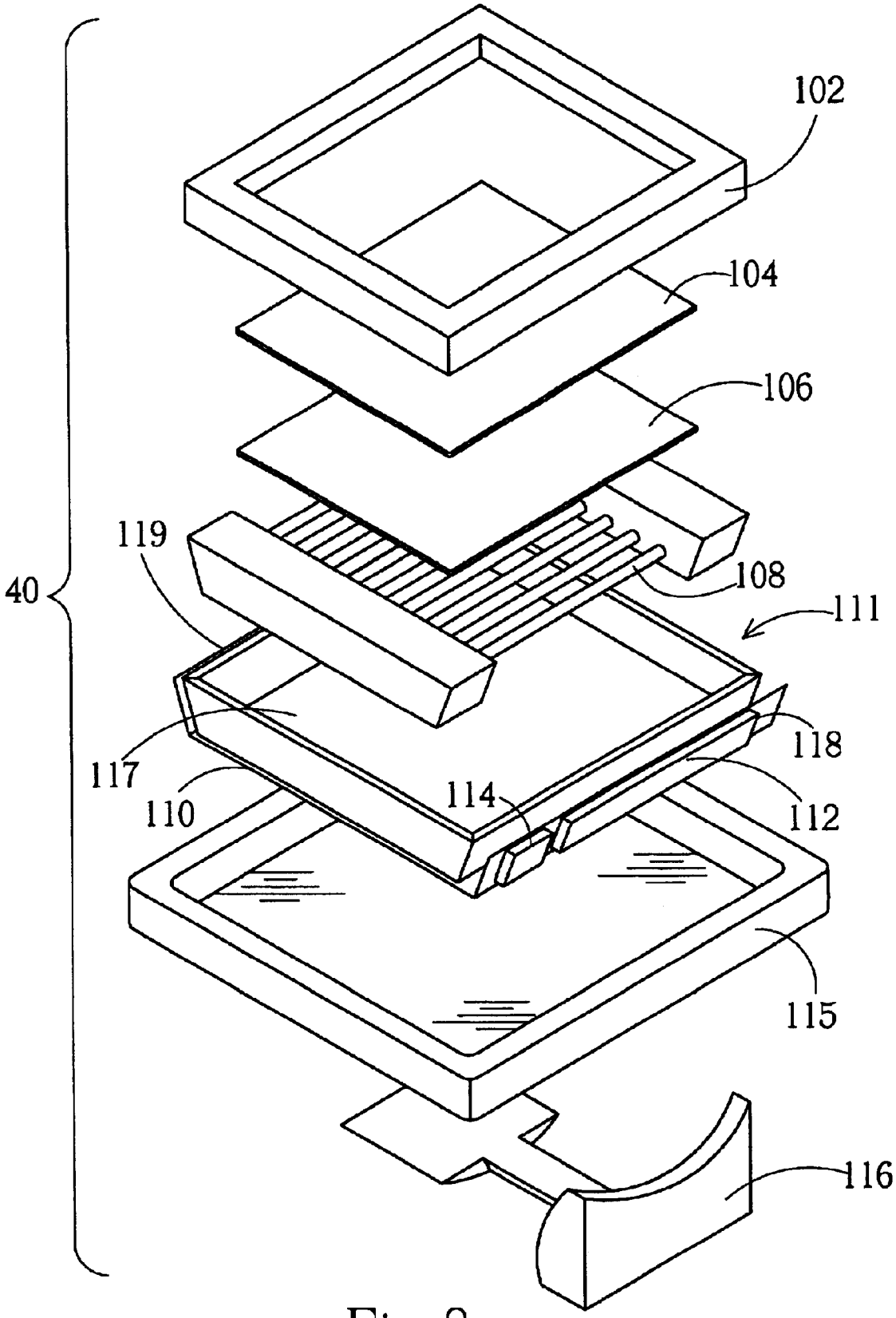
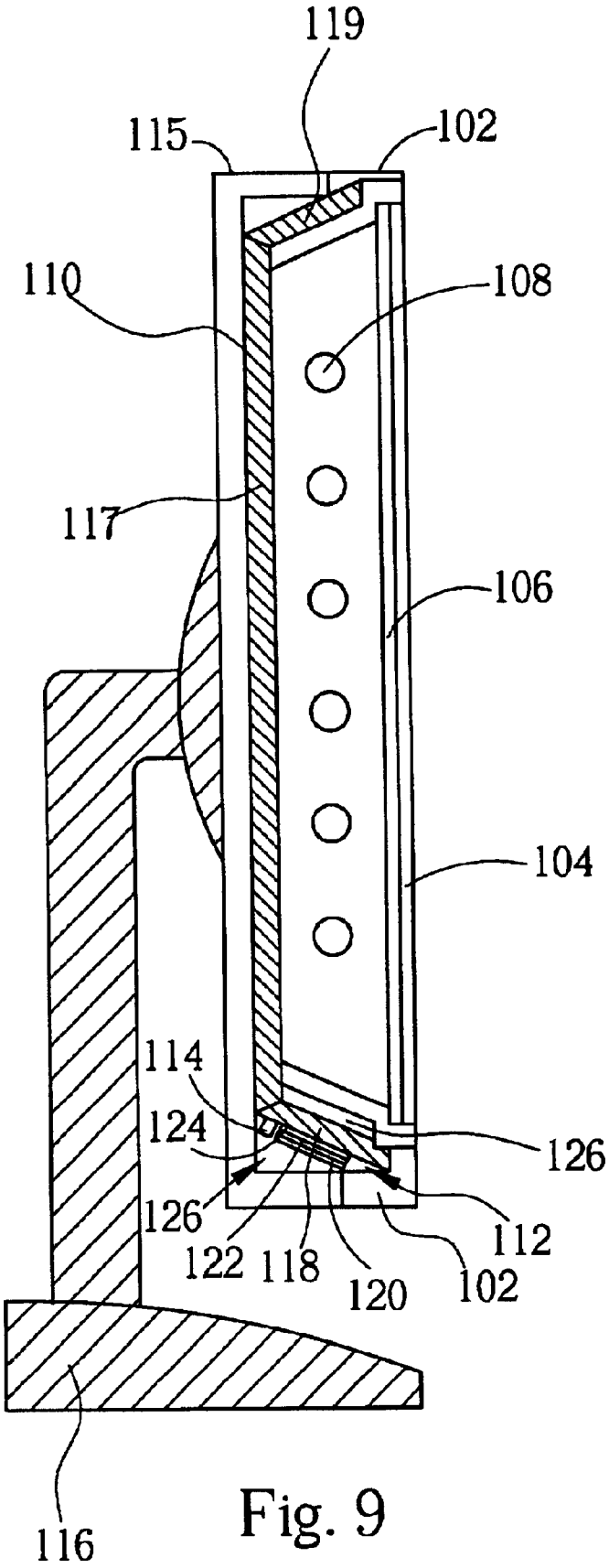


Fig. 8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102
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118
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116

Fig. 9

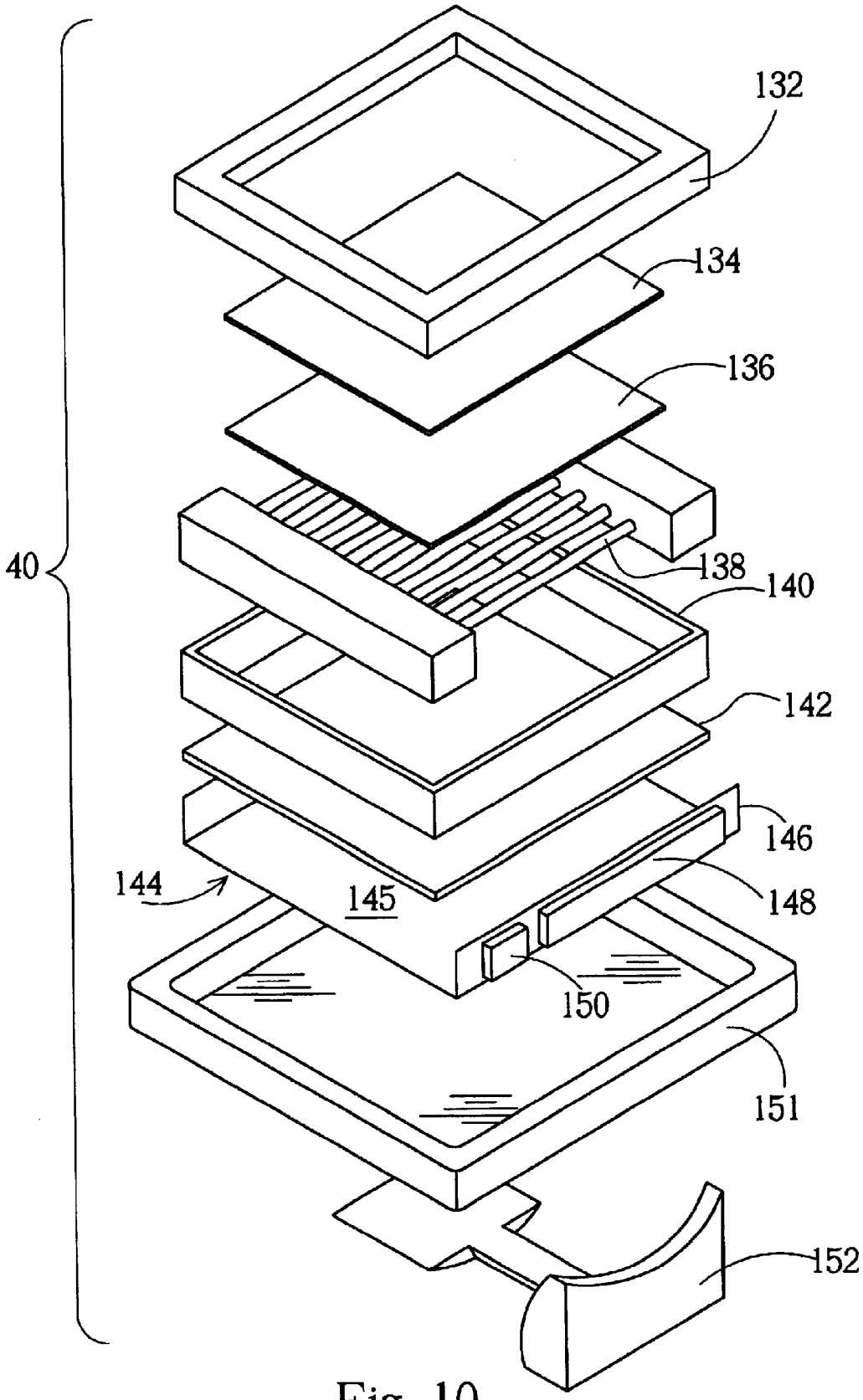

Fig. 10

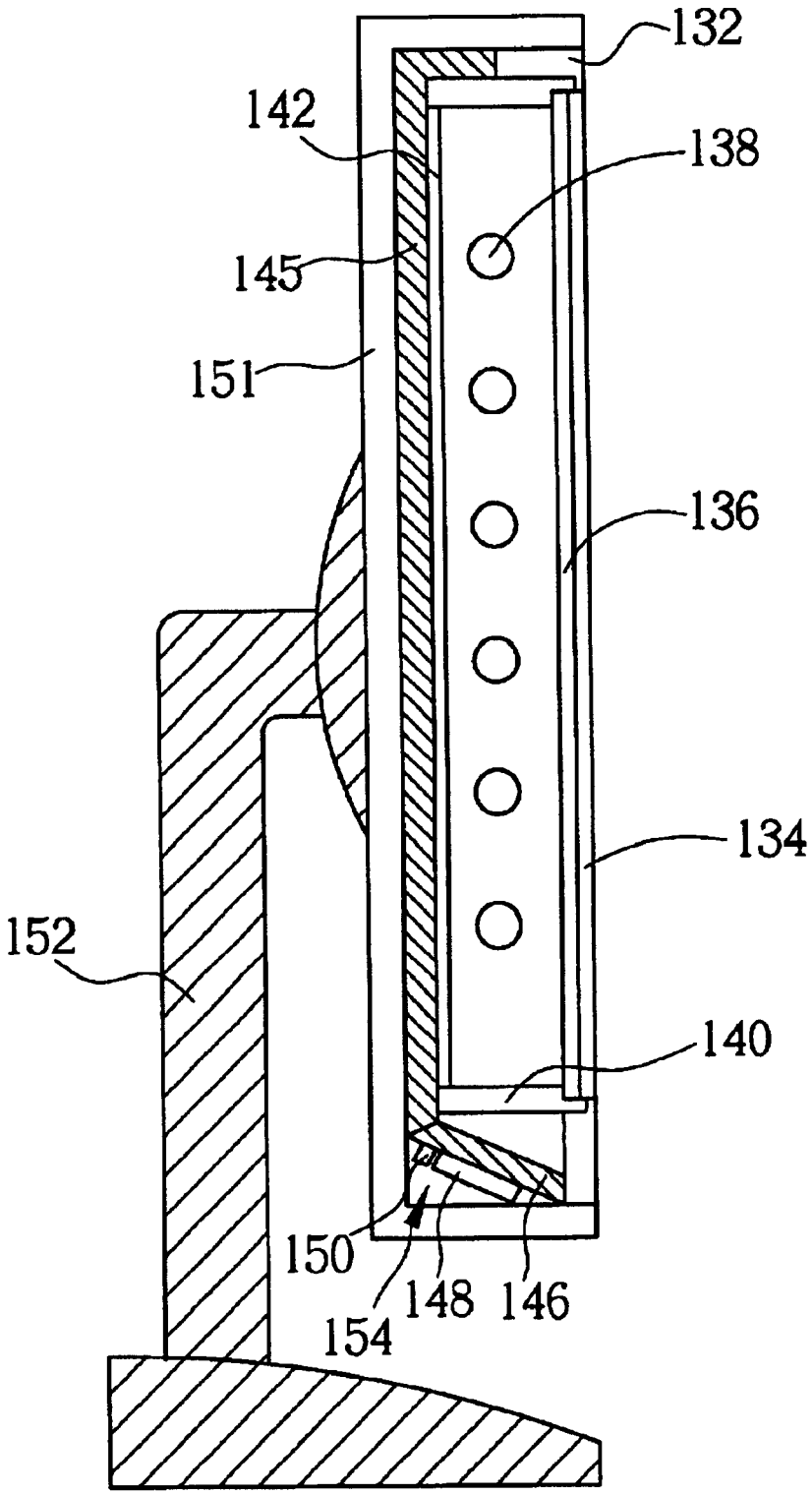

Fig. 11

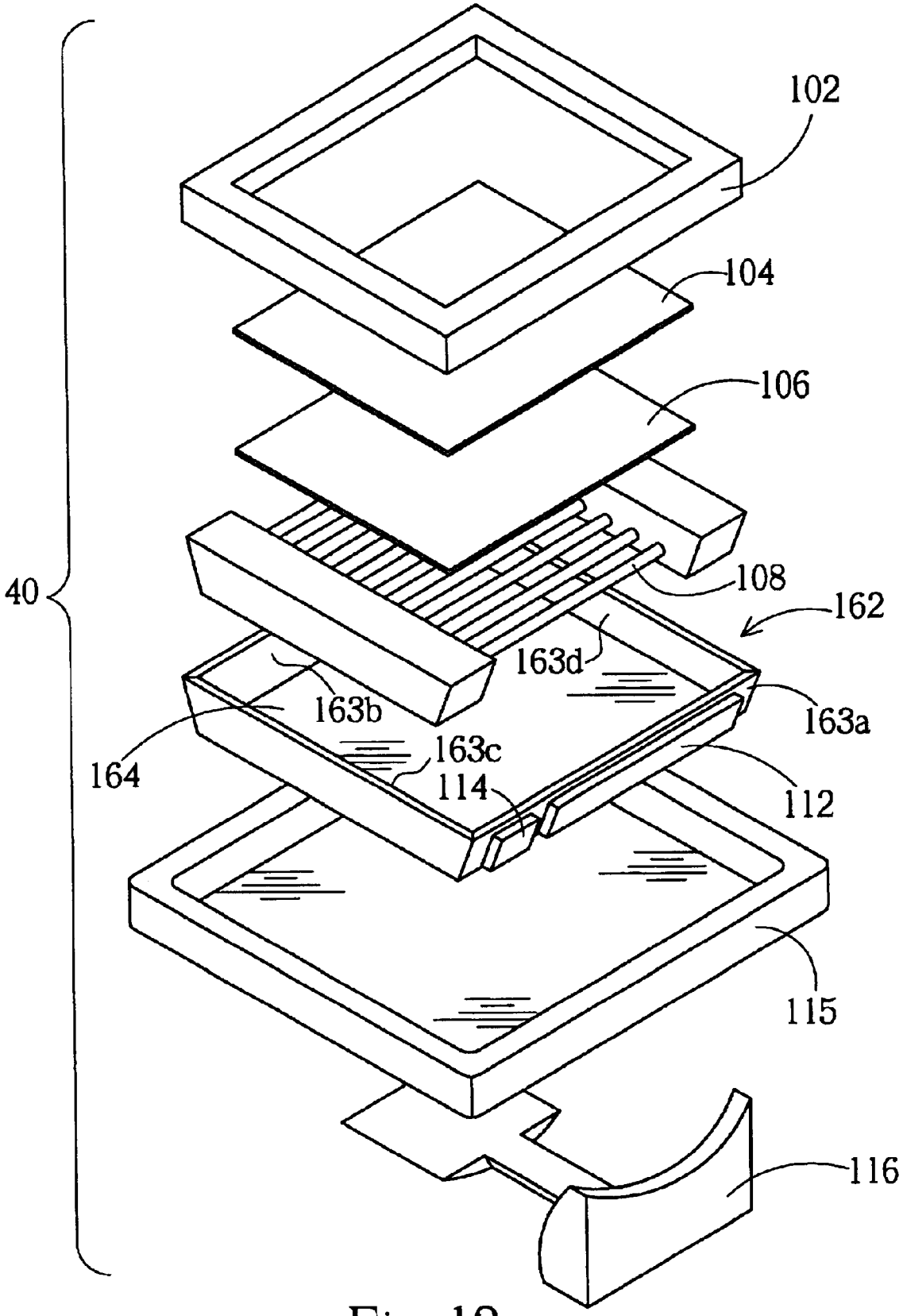

Fig. 12

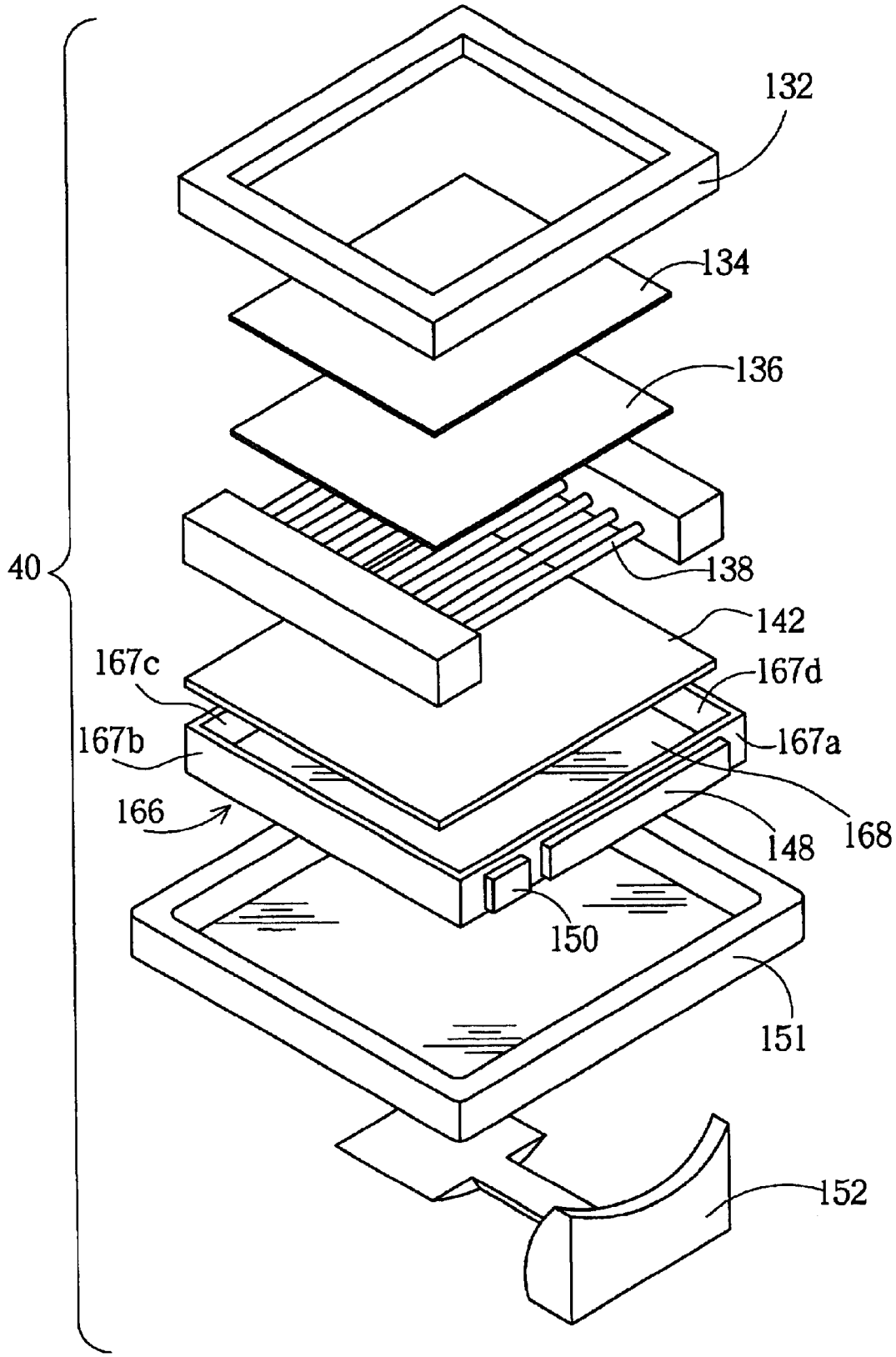
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Fig. 13

DISPLAY APPARATUS WITH A REDUCED THICKNESS

BACKGROUND OF INVENTION

1. Field of the Invention

The present invention relates to a Liquid Crystal Display (LCD) apparatus with a reduced thickness, and more specifically, to an LCD apparatus with no control circuit board installed onto the back of the back light unit.

2. Description of the Prior Art

As technology advances, computers are extensively utilized by home users as well as within companies. With the coming of age of multimedia technology, personal computers now have exceptional graphical capabilities, making a monitor one of the most important components of a personal computer system.

Currently, the most popular types of monitors are Cathode Ray Tube (CRT) monitors and LCD monitors. CRT monitors employ electron beams to excite fluorescent material to generate an image. Accordingly, CRT monitors have high power consumption for generating the electron beams, and require a large volume to accommodate the CRT itself. Monitors of larger screen size require larger bodies to accommodate the CRTs, and this often leads to an inconvenience for the user. In addition, CRT monitors generate electromagnetic radiation when displaying images and this affects users health. Due to the aforementioned issues, LCD monitors are gradually becoming embraced by computer users as mainstream products, and as replacements for CRT monitors. Not only do LCD monitors use less space, they also consume less power. Furthermore, LCD monitors do not generate enough electromagnetic radiation to be a user health concern.

Among various types of LCD apparatuses, direct-type LCD apparatuses, such as direct-type LCD monitors and televisions, are broadly used as large-size display.

Please refer to FIG. **1**, which illustrates the constituent components of a well-known direct-type LCD monitor **10**. The LCD monitor **10** comprises an upper frame **12** and a lower frame **24** which hold in place the internal components of the LCD monitor **10**. The internal components comprise an LCD panel **14** for displaying images, a diffuser **18** to equalize light, a light tube array **20** to generate white light, and a reflecting plate **22** to reflect the light generated by the light tube array **20**. A stand assembly **25** is also included to support the LCD monitor **10**. When the light emitted by the light tube array **20** shines directly onto the diffuser **18** or is reflected by the reflecting plate **22** before reaching the diffuser **18**, the diffuser **18** equalizes the light so that the light provides uniform illumination to the LCD panel **14**.

FIG. **2** shows the back of the reflecting plate **22** shown in FIG. **1**. On the back of the reflecting plate **22** are an X-board **30** and a Y-board **32** electrically connected to the LCD panel **14**, an analog-to-digital converter (A/D board) **34** to convert analog signals into digital signals, a control board **35** connected to X-board **30** and Y-board **32**, and a connector **36** connected to the A/D board **34**. The connector **36** receives signals sent from an imaging device such as a computer video card. The signals are then converted to digital signals via the A/D board **34** that are then fed into the control board **35**. The control board **35** generates corresponding signals for the X-board **30** and the Y-board **32**. The X-board **30** and the Y-board **32** then generate corresponding control signals for the LCD panel **14** to display images.

In those direct-type LCD apparatuses, a light tube array **20** illuminates the display panel **14** with no bulky light guide plate and hence the weight of the apparatuses is reduced. However, employing the light tube array **20** requires enough space for diffusion of the light, which rules out the possibility of further slimming direct-type LCD apparatuses in this regard. Besides, existing technology is implemented in such a way that the control elements are installed between reflecting plate **22** and lower frame **24**, so that the thickness of the LCD apparatus is increased, which causes inconveniences in using and installing.

SUMMARY OF INVENTION

It is therefore a primary objective of the claimed invention to provide a display apparatus with reduced thickness to solve the abovementioned problems of the prior art.

The first preferred embodiment of the claimed invention includes a display apparatus, which comprises an upper frame, a display panel installed in the upper frame to display images, a light tube array behind the display panel to generate light, a reflecting plate disposed behind the light tube array to reflect the light generated by the light tube array, and a supporting frame installed on the reflecting plate to support the display panel. The reflecting plate comprises a main portion and at least one side portion, each the of side portions tilted with respect to the main portion. The display apparatus also comprises a circuit board attached to at least one side portion of the reflecting plate and installed within the gap between the side portion of the reflecting plate and the supporting frame in order to control the operation of the display apparatus.

The second preferred embodiment of the claimed invention includes an display apparatus, which comprises an upper frame, a display panel installed inside the upper frame for displaying images, an array of light tubes disposed behind the display panel for generating light, a reflecting sheet positioned behind the array of light tubes for reflecting light generated by the array of light tubes, a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, a supporting frame positioned onto the main portion of the supporting plate for supporting the display panel, and a circuit board for controlling operations of the display apparatus. The main portion of the supporting plate is used for supporting the reflecting sheet. The supporting frame has a plurality of sub-frames, and at least one of the sub-frames is tilted with respect to the main portion of the supporting plate and is separated from the side portion of the supporting plate by a gap. The circuit board is installed within the gap.

The third preferred embodiment of the claimed invention includes an display apparatus, which comprises an upper frame, a display panel installed inside the upper frame to display images, a light tube array behind the display panel to generate light, a reflecting plate placed at the back of the light tube array to reflect the light generated by the light tube array, a supporting frame installed on the reflecting plate to support the display panel, and a lower frame. The reflecting plate comprises a main portion and at least one side portion, each the of side portions tilted with respect to the main portion. The display apparatus also comprises a circuit board attached to at least one side-portion of the reflecting plate and installed within the gap between the side portion of the reflecting plate and the lower frame in order to control the operation of the display apparatus.

The fourth preferred embodiment of the claimed invention includes andisplay apparatus, which comprises an upper

frame, a display panel installed inside the upper frame for displaying images, an array of light tubes disposed behind the display panel for generating light, a reflecting sheet positioned behind the array of light tubes for reflecting light generated by the array of light tubes, a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, a supporting frame positioned onto the main portion of the supporting plate for supporting the display panel, a lower frame, and a circuit board for controlling operations of the display apparatus. The main portion of the supporting plate is used for supporting the reflecting sheet. The supporting frame has a plurality of sub-frames, and at least one of the sub-frames is tilted with respect to the main portion of the supporting plate. The circuit board is installed onto at least one side portion of the supporting plate and within the gap between the side porting of the supporting plate and the lower frame.

It is an advantage of the claimed invention, in which no circuit board is installed on the back side of the direct-type back light unit, such that the display apparatus has a simplified frame structure and is therefore slimmer and more convenient to use. It is a further advantage of the claimed invention that production cost of the display apparatus is greatly reduced.

These and other objectives of the claimed invention will no doubt become obvious to those of ordinary skill in the art after reading the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

BRIEF DESCRIPTION OF DRAWINGS

FIG. **1** is an exploded perspective view of a prior art direct-type LCD apparatus.

FIG. **2** is a perspective view of a backside of the prior art reflecting plate shown in FIG. **1**.

FIG. **3** is a perspective view of a present invention direct-type LCD apparatus.

FIG. **4** is an exploded perspective view of a first embodiment of the present invention shown in FIG. **3**.

FIG. **5** is a cross-sectional view of the first embodiment of the present invention along a line **5**–**5**" shown in FIG. **3**.

FIG. **6** is an exploded perspective view of a second embodiment of the present invention shown in FIG. **3**.

FIG. **7** is a cross-sectional view of the second embodiment of the present invention along a line **5**–**5**" shown in FIG. **3**.

FIG. **8** is an exploded perspective view of a third embodiment of the present Invention shown in FIG. **3**.

FIG. **9** is a cross-sectional view of the third embodiment of the present invention along a line **5**–**5**" shown in FIG. **3**.

FIG. **10** is an exploded perspective view of a forth embodiment of the present Invention shown in FIG. **3**.

FIG. **11** is a cross-sectional view of the forth embodiment of the present invention along a line **5**–**5**" shown in FIG. **3**.

FIG. **12** is an exploded perspective view of a fifth embodiment of the present invention shown in FIG. **3**.

FIG. **13** is an exploded perspective view of a sixth embodiment of the present invention shown in FIG. **3**.

DETAILED DESCRIPTION

Please Refer to FIG. **3**, FIG. **4**, and FIG. **5**. FIG. **3** illustrates a direct-type LCD apparatus **40** according to the present invention, and shows a section line **5**–**5**" used for FIG. **5**. FIG. **4** illustrates components of the LCD apparatus **40** according to the first embodiment of the present invention. The LCD apparatus **40** comprises anupper frame **42**, a liquid crystal display panel **44** installed inside the upper frame **42**, a light tube array **48** installed behind the display panel **44** for generating white light, a diffuser **46** interposed between the display panel **44** and the light tube array **48** in order to uniformly diffuse the light generated by the light tube array **48**, a reflecting plate **50** disposed behind the light tube array **48**, a supporting frame **51** installed on the reflecting plate **50** to support the liquid crystal display panel **44** and the diffuser **46**, a circuit board **52** to control the display panel **44**, and a connector **54** to receive signals sent by imaging devices. The reflecting plate **50** comprises a main portion **57** and two side portions **58**, **59**. Each of the side portions **58**, **59** is tilted with respect to the main portion **57**. The supporting frame **51** comprises four sub-frames **53***a*, **53***b*, **53***c*, **53***d*, among which at least sub-frames **53***a* and **53***b* are also tilted with respect to the main portion **57** so as to reflect the light generated by the light tube array **48**. In addition, sub-frame **53***a* is separated from the side portion of the reflecting plate **58** by a gap **66**.

The first preferred embodiment of the present invention utilizes the supporting frame **51** so that the LCD apparatus **40** is strengthened and capable of withstanding the effects of external forces. Moreover, the main portion **57** of the reflecting plate **50** along with the sub-frames **53***a*, **53***b*, **53***c* and **53***d* of the supporting frame **51** constitute a reflecting surface, which reflects the light generated by the light tube array **48**. The circuit board **52** comprises at least an X-board **60** to drive pixels in the same row for displaying corresponding data, a control board **62** used to control the X-board **60**, and an A/D board **64** to convert analog signals into digital signals. The circuit board **52** can be a rigid circuit board or a printed circuit board. The circuit board **52** could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board **52**. In this embodiment, the circuit board **52** of the direct-type LCD apparatus **40** is installed ontoeither the side portion **58** of the reflecting plate **57** or the sub-frame **53***a* of the supporting frame **51** by making use of the gap **66**.

In order to reduce the weight of the LCD apparatus **40**, the supporting frame **51** can be made of materials such as plastic. Additionally, by using multi-layer printed circuit board technology, all of the control boards such as the X-board **60** and the analog-to-digital converter **64** can be integrated into the single circuit board **52** through printed circuit board assembly (PCBA). Another weight saving feature is that the reflecting plate **50** forms a part of the frame of the LCD apparatus **40**. A stand assembly **56** could be further provided and coupled to either the reflecting plate **57** to support the LCD apparatus **40**. The present invention is not limited by the first preferred embodiment described. For example, one end of the stand assembly **56** can be installed on the bottom side of the upper frame **42** to support the entire LCD apparatus **40**. Additionally, the sub-frame **53***b* and the side portion **59** can also be used to form another gap with the same purpose as the gap **66** formed by the sub-frame **53***a* and the side portion **58**. Part of the circuit board **52** can then be attached to the side portion **58** reflecting plate **50** or the sub-frame **53***a*, while the rest is attached to the side portion **59** or the sub-frame **53***b*, so as to make complete use of the space between the two side portions **58**, **59** and the supporting frame **51**. Without any circuit board **52** is installed on the back side of the reflecting plate **50**, the thickness of the LCD apparatus **40** is reduced.

Please refer to FIG. **6** and FIG. **7**. FIG. **6** is an exploded perspective view of a second embodiment of the present invention and FIG. **7** is a cross-sectional view of the second

embodiment along a line 5–5" shown in FIG. 3. The LCD apparatus 40 comprises anupper frame 72, a liquid crystal display panel 74 installed inside the upper frame 72, a light tube array 78 installed behind the display panel 74 for generating white light, a diffuser 76 interposed between the liquid crystal display panel 74 and the light tube array 78 in order to uniformly diffuse the light generated by the light tube array 78, a supporting frame 80 for supporting the liquid crystal display panel 74, a reflecting sheet 82 for reflecting light generated by the light tube array 78, and a supporting plate 84 for supporting the supporting frame 80. The supporting plate 84 has a main portion 85 and at least one side portion 86. The reflecting sheet 82 is positioned onto the main portion 85. As shown in FIG. 6, the side portion 86 is tilted with respect to the main portion 85. A gap 94 exists between the side portion 86 and the supporting frame 80. The LCD apparatus further comprises a circuit board 88 for controlling the display panel 74, and a connector 90 for receiving display data sent by an external display controller such as a VGA card of a computer system. The circuit board 88 is installed within the gap 94.

In this second preferred embodiment, the circuit board 88 can be a rigid circuit board or a printed circuit board. The circuit board 88 could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 88. For example, a heatsink covering the circuit board 88 not only prevents the circuit board 88 from running under high temperature, but also functions as an electromagnetic interference shield.

As mentioned above, the circuit board 88 is installed within the gap 94 without increasing thickness of the LCD apparatus 40. Besides, for further reducing the weight, the supporting plate 84 serves a part of the frame of the LCD apparatus 40. A stand assembly 92 could be further provided and coupled to either the supporting plate 84 to support the LCD apparatus 40.

The present invention is not limited by the second preferred embodiment described. For example, one end of the stand assembly 92 can be installed on the bottom side of the upper frame 72 to support the entire LCD apparatus 40. Additionally, the gap 94 can exist in any side of the LCD apparatus 40 through appropriate arrangement of the side portion 86. For example, when the side portion 86 is positioned on the top of the main portion 85, the gap 94 will exist on the top of the LCD apparatus 40. In addition, the supporting plate 84 can have more than one side portion 86 for accommodating more circuit boards 88 to better drive the LCD apparatus 40 without increasing its corresponding thickness and weight. The alternative arrangement also can achieve the same goal of reducing the thickness of the prior art LCD apparatus 10.

Please Refer to FIG. 8, and FIG. 9. FIG. 8 illustrates components of the LCD apparatus 40 according to the third embodiment of the present invention. FIG. 9 is a cross-sectional view of the LCD apparatus 40. The LCD apparatus 40 comprises an upper frame 102, a liquid crystal display panel 104 installed inside the upper frame 102, a light tube array 108 installed behind the display panel 104 for generating white light, a diffuser 106 interposed between the display panel 104 and the light tube array 108 in order to uniformly diffuse the light generated by the light tube array 108, a reflecting plate 110 disposed behind the light tube array 108, a supporting frame 111 installed on the reflecting plate 110 to support the liquid crystal display panel 104 and the diffuser 106, a circuit board 112 to control the display panel 104, a connector 114 to receive signals sent by imaging devices, and a lower frame 115. The reflecting plate 110 comprises a main portion 117 and two side portions 118, 119. Each of the side portions 118, 119 is tilted with respect to the main portion 117. The main portion 117 of the reflecting plate 110 along with the supporting frame 111 constitute a reflecting surface, which reflects the light generated by the light tube array 108. It is noteworthy that a gap 126 exists between the side portion 118 and the lower frame 115. Then, the circuit board 112 is installed within the gap 126. The circuit board 112 comprises at least an X-board 120 to drive pixels in the same row for displaying corresponding data, a control board 122 used to control the X-board 120, and an A/D board 124 to convert analog signals into digital signals. The circuit board 112 can be a rigid circuit board or a printed circuit board. The circuit board 112 could also Include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 112. In this embodiment, the circuit board 112 and connector 114 are installed onto the side portion 118 of the reflecting plate 110 and protected by the lower frame 115. The lower frame 115 could be any shape and size to provide protection and/or shield for the circuit board 112 and is not limited to a lower housing case to enclose the whole reflecting plate 110 and supporting frame 111. A stand assembly 116 could be further provided and coupled to either the reflecting plate 117 or the lower frame 115 to support the LCD apparatus 40. Without any circuit board 112 is installed on the back of the reflecting plate 110, the thickness of the LCD apparatus 40 is reduced.

Please refer to FIG. 10 and FIG. 11. FIG. 10 is an exploded perspective view of a fourth embodiment of the present invention and FIG. 11 is a cross-sectional view of the forth embodiment along a line 5–5" shown in FIG. 3. The LCD apparatus 40 comprises an upper frame 132, a liquid crystal display panel 134 installed inside the upper frame 132, a light tube array 138 installed behind the display panel 134 for generating white light, a diffuser 136 interposed between the liquid crystal display panel 134 and the light tube array 138 in order to uniformly diffuse the light generated by the light tube array 138, a supporting frame 140 for supporting the liquid crystal display panel 134, a reflecting sheet 142 for reflecting light generated by the light tube array 138,and a supporting plate 144 for supporting the supporting frame 140. The supporting plate 144 has a main portion 145 and at least one side portion 146. The reflecting sheet 142 is positioned onto the main portion 145. The LCD apparatus 40 further comprises a circuit board 148 and a connector 150 installed onto the side portion 146 and protected by a lower frame 151. It is noteworthy that a gap 154 exists between the side portion 146 and the lower frame 151. Then, the circuit board 148 is installed within the gap 156. The circuit board 148 could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board 148. For example, a heatsink covering the circuit board 148 not only prevents the circuit board 148 from running under high temperature, but also functions as an electromagnetic interference shield. The lower frame 151 could be any shape and size to provide protection and/or shield for the circuit board 148 and is not limited to a lower housing case to enclose the whole supporting plate 144 and supporting frame 140. A stand assembly 152 could be further provided and coupled to either the supporting plate 144 or the lower frame 151 to support the LCD apparatus 40. Without any circuit board 148 installed on the back side of the reflecting plate 144, the thickness of the LCD apparatus 40 is reduced.

Please Refer to FIG. 12, which illustrates components of the LCD apparatus 40 according to a fifth embodiment of the present invention. The only difference between this fifth

embodiment and the third embodiment is that the reflecting plate **110** shown in FIG. **8** incorporates the supporting frame **111** shown in FIG. **8** to form an integrated supporting unit **162**. The integrated supporting unit **162** further simplifies the whole structure of the LCD apparatus **40**, and accordingly reduces thickness and cost of the LCD apparatus **40**. The integrated supporting unit **162** comprises four sub-frames **163***a*, **163***b*, **163***c*, **163***d* and a main portion **164**. The sub-frames **163***a*, **163***b*, **163***c*, **163** are mainly used to make the LCD apparatus **40** firm and solid. The main portion **164** is mainly used to reflect light generated by the light tube array **108**. In other words, the integrated supporting unit **162** in the fifth embodiment has two functions originally provided by the reflecting plate **110** and the supporting frame **111**. The connector **114** and the circuit board **112**, therefore, are positioned onto one of the sub-frames **113***a*, **113***b*, **113***c*, **113***d* (the sub-frame **113***a* for example). It is noteworthy that the circuit board **112** could also include an electromagnetic interference shield to shield the electromagnetic radiation generated by the circuit board **112**. For example, a heatsink covering the circuit board **112** not only prevents the circuit board **112** from running under high temperature, but also functions as an electromagnetic interference shield. In addition, the stand assembly **116** is coupled to lower frame **116** to support the LCD apparatus **40**.

Please refer to FIG. **13**, which illustrates components of the LCD apparatus **40** according to a sixth embodiment of the present invention. The only difference between this sixth embodiment and the forth embodiment is that the supporting plate **144** shown in FIG. **10** incorporates the supporting frame **140** shown in FIG. **10** to form an integrated supporting unit **166**. The integrated supporting unit **166** further simplifies the whole structure of the LCD apparatus **40**, and accordingly reduces thickness and cost of LCD apparatus **40**. The integrated supporting unit **166** comprises four sub-frames **167***a*, **167***b*, **167***c*, **167***d* and a main portion **168**. The integrated supporting unit **166** is mainly used to make the LCD apparatus **40** firm and solid. The reflecting sheet **142** for reflecting light generated by the light tube array **138** is positioned onto the main portion **168**. The connector **150** and the circuit board **148**, therefore, are both positioned onto one of the sub-frames **167***a*, **167***b*, **167***c*, **167***d* (sub-frame **167***a* for example). It is noteworthy that the circuit board **148** could also include an electromagnetic Interference shield to shield the electromagnetic radiation generated by the circuit board **148**. For example, a heatsink covering the circuit board **148** not only prevents the circuit board **148** from running under high temperature, but also functions as an electromagnetic interference shield. In addition, the stand assembly **152** is coupled to the lower frame **152** to support the LCD apparatus **40**.

As shown in FIG. **8** and FIG. **12**, the stand assembly **116** is fixed on the lower frame **115**. However, the stand assembly **116** is capable of piercing through the lower frame **155** to connect with the reflecting plate **110** (third embodiment) or the integrated supporting unit **162** (fifth embodiment). The reflecting plate **110** and the stand assembly **116**, therefore, are coupled together to support the LCD apparatus **40**. The integrated supporting unit **162** and the stand assembly **116** are connected to support the LCD apparatus **40** in the same way. As shown in FIG. **10** and FIG. **13**, the stand assembly **152** is fixed on the lower frame **151**. However, the stand assembly **152** is capable of piercing through the lower frame **151** to connect with the supporting plate **144** (fourth embodiment)or the integrated supporting unit **166** (sixth embodiment). The supporting plate **144** and the stand assembly **152**, therefore, are coupled together to support the LCD apparatus **40**. The Integrated supporting unit **166** and the stand assembly **152** are connected to support the LCD apparatus **40** in the same way.

Compared with the prior art direct-type LCD apparatus, the present invention utilizes the space between the side portions of the reflecting plate and the supporting frame (first preferred embodiment), the side portions of the supporting plate and the supporting frame (second preferred embodiment), the side portion of the supporting plate and the lower frame**9**third and fifth embodiments), or the side portion of the reflecting plate and the lower frame (fourth and sixth embodiments) to house the circuit board and related elements. As a result, the thickness of the direct-type LCD apparatus is reduced without the circuit board and related elements positioned at the back of the LCD apparatus. Therefore, it makes the LCD apparatus more convenient to use. Furthermore, the present invention utilizes the main portion of the reflecting plate (first preferred embodiment) or the supporting plate (second preferred embodiment) as a frame structure to replace the lower frame of the prior art LCD apparatus. The entire apparatus is supported by the stand assembly in combination with the main portion of the reflecting plate or the main portion of the supporting plate. No extra lower frames are required to protect the circuit board and support the apparatus. Accordingly, the overall production cost and weight of the LCD apparatus are greatly reduced.

Those skilled in the art will readily observe that numerous modifications and alterations of the device may be made while retaining the teachings of the invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.

What is claimed is:

1. A display apparatus comprising:

an upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;

a supporting frame installed on the reflecting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the reflecting plate and being separated from the side portion by a gap; and

a circuit board installed within the gap for controlling operations of the display apparatus.

2. The display apparatus of claim **1** wherein the display panel is a liquid crystal display panel.

3. The display apparatus of claim **1** further comprising a stand assembly having one end coupled to the reflecting plate.

4. The display apparatus of claim **1** further comprising a stand assembly having one end coupled to the upper frame.

5. The display apparatus of claim **1** further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

6. The display apparatus of claim **1** further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation.

7. The display apparatus of claim 1 wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

8. A display apparatus comprising:

an upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

a reflecting sheet disposed behind the array of light tubes for reflecting light generated by the array of light tubes;

a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, the main portion used for supporting the reflecting sheet;

a supporting frame disposed on the supporting plate for supporting the display panel, the supporting frame comprising a plurality of sub-frames, at least one of the sub-frames being tilted with respect to the main portion of the supporting plate and being separated from the side portion of the supporting plate by a gap; and

a circuit board installed within the gap for controlling operations of the display apparatus.

9. The display apparatus of claim 8 wherein the display panel is a liquid crystal display panel.

10. The display apparatus of claim 8 further comprising a stand assembly having one end coupled to the supporting plate.

11. The display apparatus of claim 8 further comprising a stand assembly having one end coupled to the upper frame.

12. The display apparatus of claim 8 further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

13. The display apparatus of claim 8 further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation.

14. The display apparatus of claim 8 wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

15. A display apparatus comprising:

an upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

a reflecting plate disposed behind the array of light tubes for reflecting light generated by the array of light tubes, the reflecting plate having a main portion and at least one side portion being tilted with respect to the main portion;

a supporting frame installed on the reflecting plate for supporting the display panel; and

a circuit board installed on the side portion of the reflecting plate for controlling operations of the display apparatus.

16. The display apparatus of claim 15 wherein the display panel is a liquid crystal display panel.

17. The display apparatus of claim 15 further comprising a stand assembly having one end coupled to the reflecting plate.

18. The display apparatus of claim 15 further comprising a stand assembly having one end coupled to the upper frame.

19. The display apparatus of claim 15 further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

20. The display apparatus of claim 15 further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation.

21. The display apparatus of claim 15 wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

22. A display apparatus comprising:

a upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

a reflecting sheet disposed behind the array of light tubes for reflecting light generated by the array of light tubes;

a supporting plate having a main portion and at least one side portion being tilted with respect to the main portion, the main portion used for supporting the reflecting sheet;

a supporting frame installed on the main portion of the supporting plate for supporting the display panel; and

a circuit board installed on the side portion of the supporting plate for controlling operations of the display apparatus.

23. The display apparatus of claim 22 wherein the display panel is a liquid crystal display panel.

24. The display apparatus of claim 22 further comprising a stand assembly having one end coupled to the supporting plate.

25. The display apparatus of claim 22 further comprising a stand assembly having one end coupled to the upper frame.

26. The display apparatus of claim 22 further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

27. The display apparatus of claim 22 further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation emitted by the circuit board.

28. The display apparatus of claim 22 wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

29. A display apparatus comprising:

an upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

an integrated supporting unit disposed behind the array of light tubes having a main portion and at least one side portion being tilted with respect to the main portion for reflecting light generated by the array of light tubes and supporting the display panel; and

a circuit board installed on at least one of the side portions of the reflecting plate for controlling operations of the display apparatus.

30. The display apparatus of claim 29 wherein the display panel is a liquid crystal display panel.

31. The display apparatus of claim 29 further comprising a stand assembly having one end coupled to the integrated supporting unit.

32. The display apparatus of claim **29** further comprising a stand assembly having one end coupled to the upper frame.

33. The display apparatus of claim **29** further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

34. The display apparatus of claim **29** further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation.

35. The display apparatus of claim **29** wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

36. A display apparatus comprising:

an upper frame;

a display panel installed inside the upper frame for displaying images;

an array of light tubes disposed behind the display panel for generating light;

a reflecting sheet disposed behind the array of light tubes for reflecting light generated by the array of light tubes;

an integrated supporting unit comprising a main portion and at least one side portion being tilted with respect to the main portion for supporting the reflecting sheet and the display panel; and

a circuit board installed on at least one of the side portions of the supporting plate for controlling operations of the display apparatus.

37. The display apparatus of claim **36** wherein the display panel is a liquid crystal display panel.

38. The display apparatus of claim **36** further comprising a stand assembly having one end coupled to the integrated supporting unit.

39. The display apparatus of claim **36** further comprising a stand assembly having one end coupled to the upper frame.

40. The display apparatus of claim **36** further comprising a diffuser interposed between the display panel and the array of light tubes for diffusing light generated by the array of light tubes.

41. The display apparatus of claim **36** further comprising an EMI (electromagnetic interference) shield covering the circuit board for shielding radiation emitted by the circuit board.

42. The display apparatus of claim **36** wherein the circuit board comprises an X-board for driving the display panel, a control board for controlling the X-board, and an A/D converter for converting analog signals into digital signals.

* * * * *

CERTIFICATE OF SERVICE

The undersigned counsel certifies that, on May 22, 2007, he electronically filed the foregoing document with the Clerk of the Court using CM/ECF, which will send automatic notification of the filing to the following:

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